

LCD-1

IVY Bridge (rPGA989)

Intel PCH (Panther Point)

DY:No stuff
SWG:SWG SKU

PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.

BOM1

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Title

Cover Page

Size
A3

Document Number

CD1 DIS

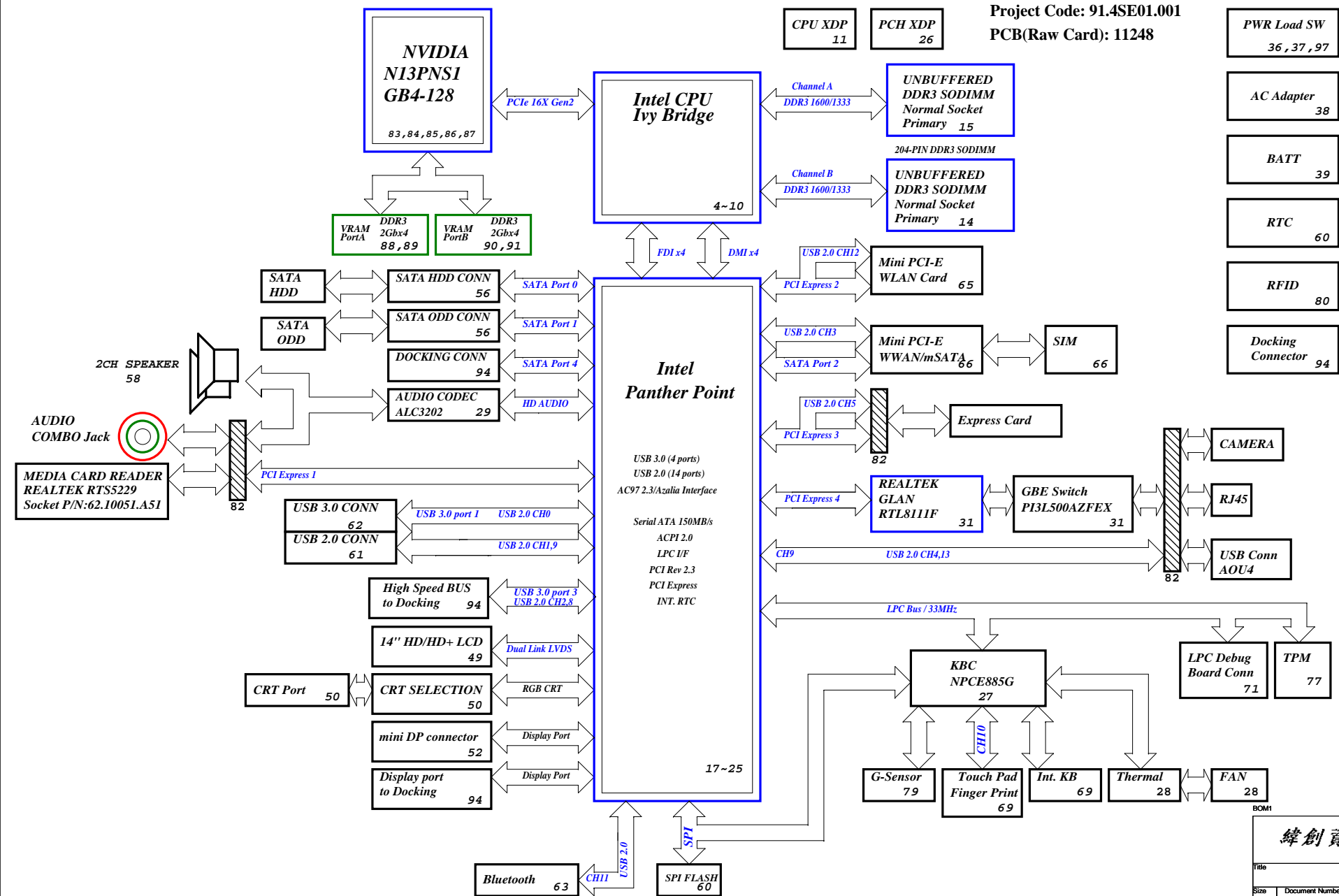
Rev

SC

Date: Tuesday, December 13, 2011

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LCD-1 Discrete Block Diagram



PCB Layer Stackup

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOTTOM

Battery Charger	
BQ24707	40
INPUTS	OUTPUTS
AD+	BT+
System DC/DC	
TPPS1123RGER	41
DCBATOUT	5V_S5 3D3V_S5
CPU DC/DC	
ISL95838HRTZ	42, 43
DCBATOUT	VCC_CORE
ID05V_VTT	
TPPS1219RTER	45
DCBATOUT	ID05V_VTT
ID5V_S3/DDR3_REF	
0D75V_S0 TPPS1216RUKR	46
DCBATOUT	0D75V_S0 ID5V_PWR DDR3_VREF
ID8V_S0	
TPPS1311RGTR	47
3D3V_S5	ID8V_S0
VCCSA	
TPPS1461RGER	48
5V_S5	VCCSA
VGA_CORE	
ISL62882CHRTZ	92
DCBATOUT	VGA_CORE

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		Block Diagram	
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PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT{3:0}# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO{33}	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPI015	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPI08	GPI08 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPI027	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

RESISTOR

Symbol name	Value	Tolerance	Rating	Size
		(J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	0402<= 1/16W, 25V 0603 >= 1/16W, 75V 0805 >= 1/10W, 100V	2<=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

CAPACITOR

Symbol name	Value	Tolerance	Rating	Size
		(M: +/-20, K: +/-10, Z: +80/-20)		2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG{2}	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG{4}		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG{6:5}	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG{7}	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
ACTIVE IN				
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA G075V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail	
5V_USBX_S3 1D5V_S3 D0K_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only	
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever IAMT is active	
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iMTLegacy WOL	
3D3V_AUX_XBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states	
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx	

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

SMBus ADDRESSES

I 2 C / SMBus Addresses	Ref Des	Chief River CRV		
Device		Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SMI1_CLK/SMI1_DATA SMI1_CLK/SMI1_DATA SMI1_CLK/SMI1_DATA
PCH SMBus SO-DIMM0 (SPD) SO-DIMM0 (SPD) SO-DIMM0 (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

PCIe Routing

LANE1	Card Reader
LANE2	Mini Card1(WLAN)
LANE3	Express Card
LANE4	GBE LAN
LANE5	X
LANE6	X
LANE7	X
LANE8	X

USB Table

Pair	Device
0	USB3.0 port 0
1	USB2.0 port 1
2	USB2.0 Docking
3	WWAN
4	USB2.0 port (AU04)
5	New Card
6	X
7	X
8	USB2.0 Docking
9	USB2.0 port 2
10	FPR
11	BLUETOOTH
12	WLAN
13	Camera

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	mSATA
3	N/A
4	Docking
5	N/A

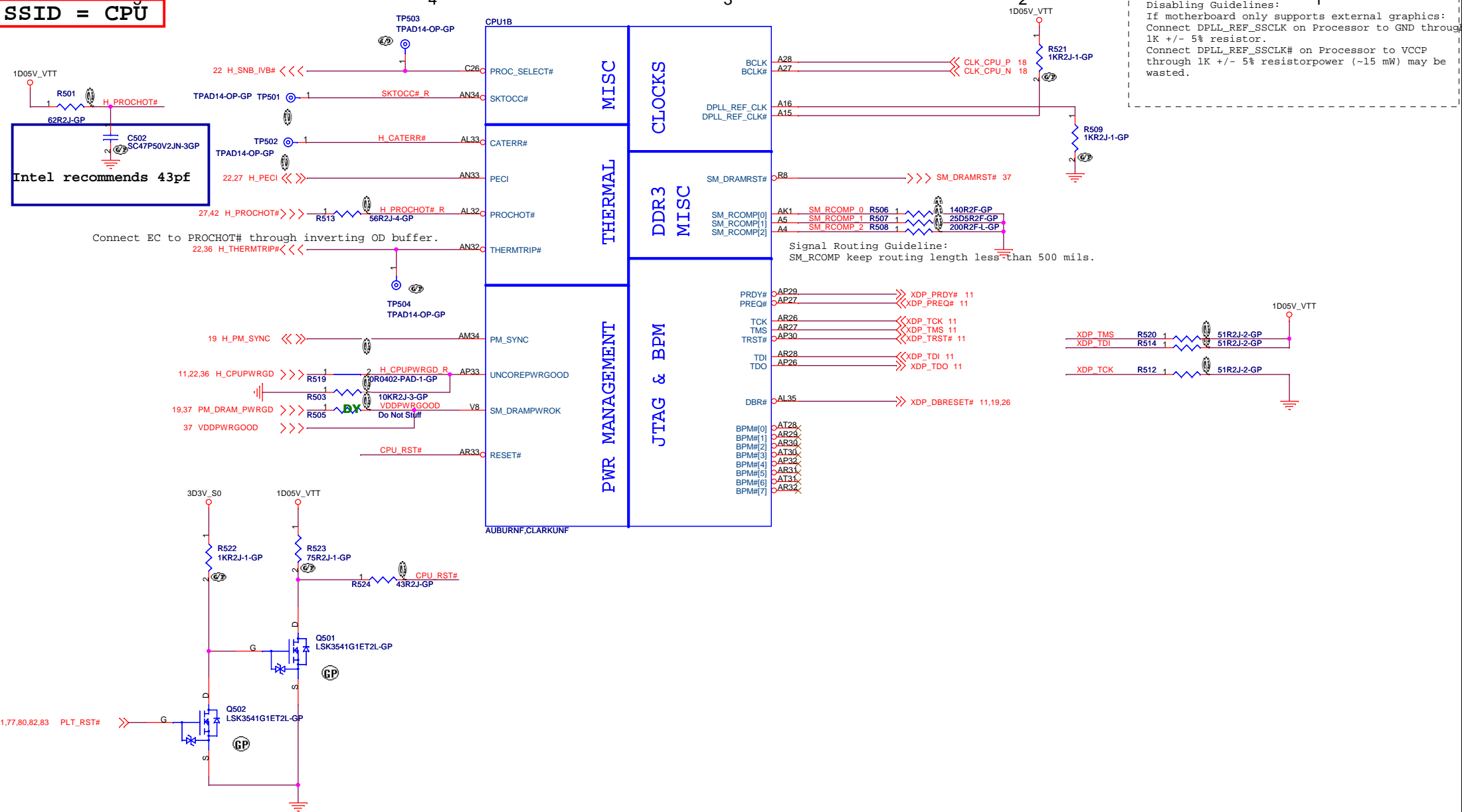
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Title			
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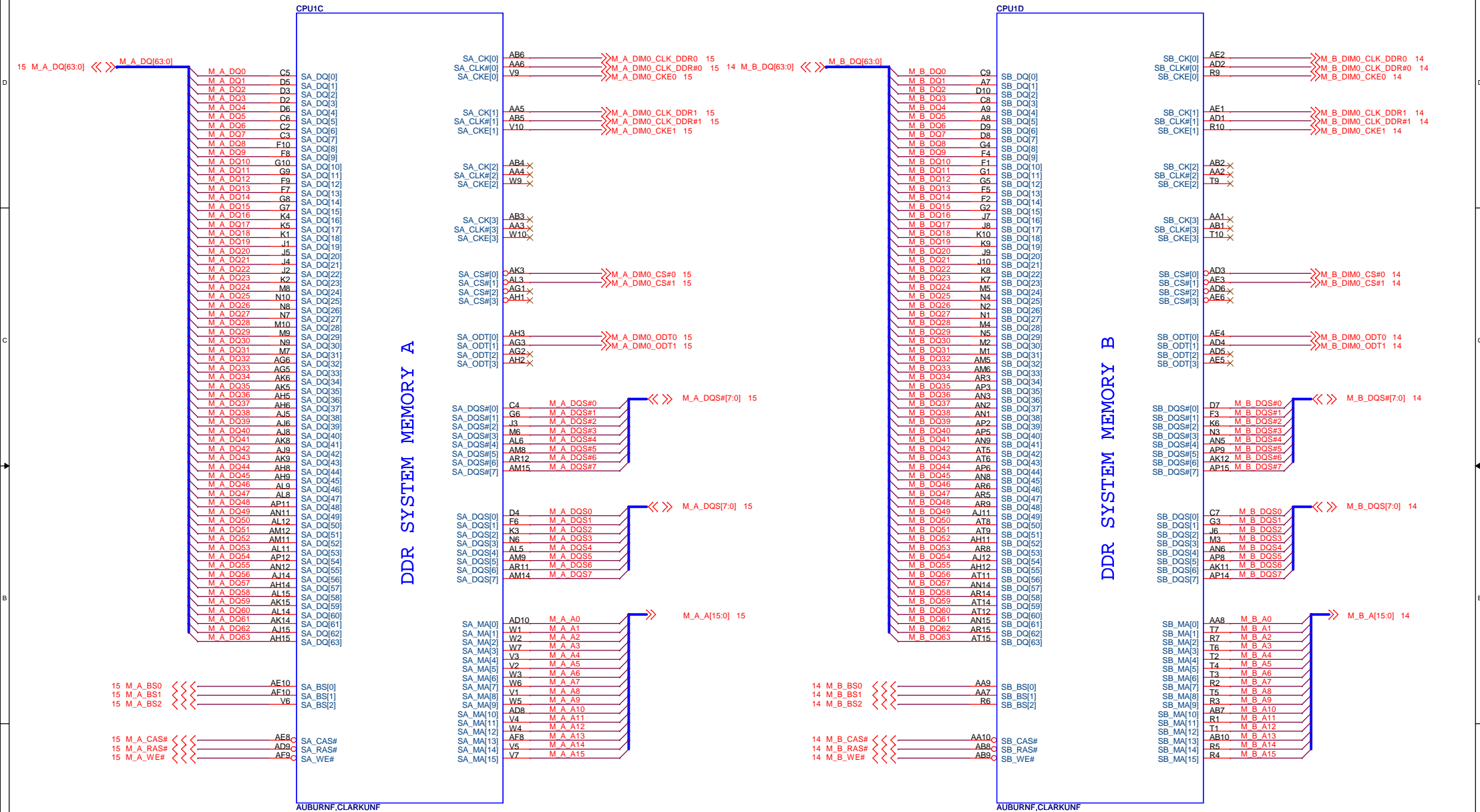
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SSID = CPU



SSID = CPU



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Title

CPU (DDR)

Size
A3

Document Number

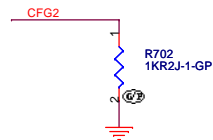
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Rev
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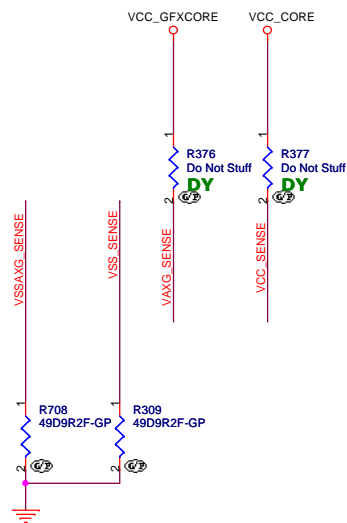
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SSID = CPU

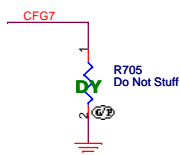


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

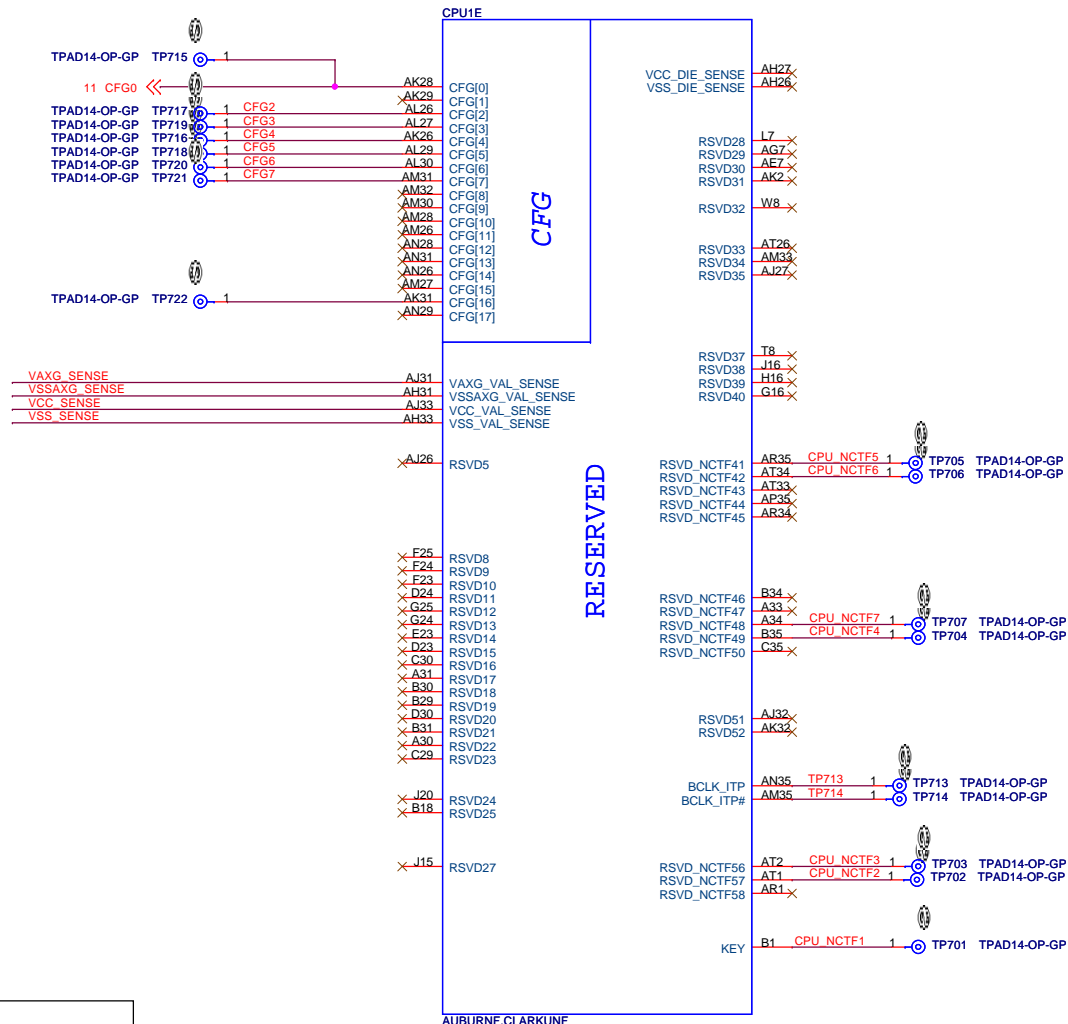
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

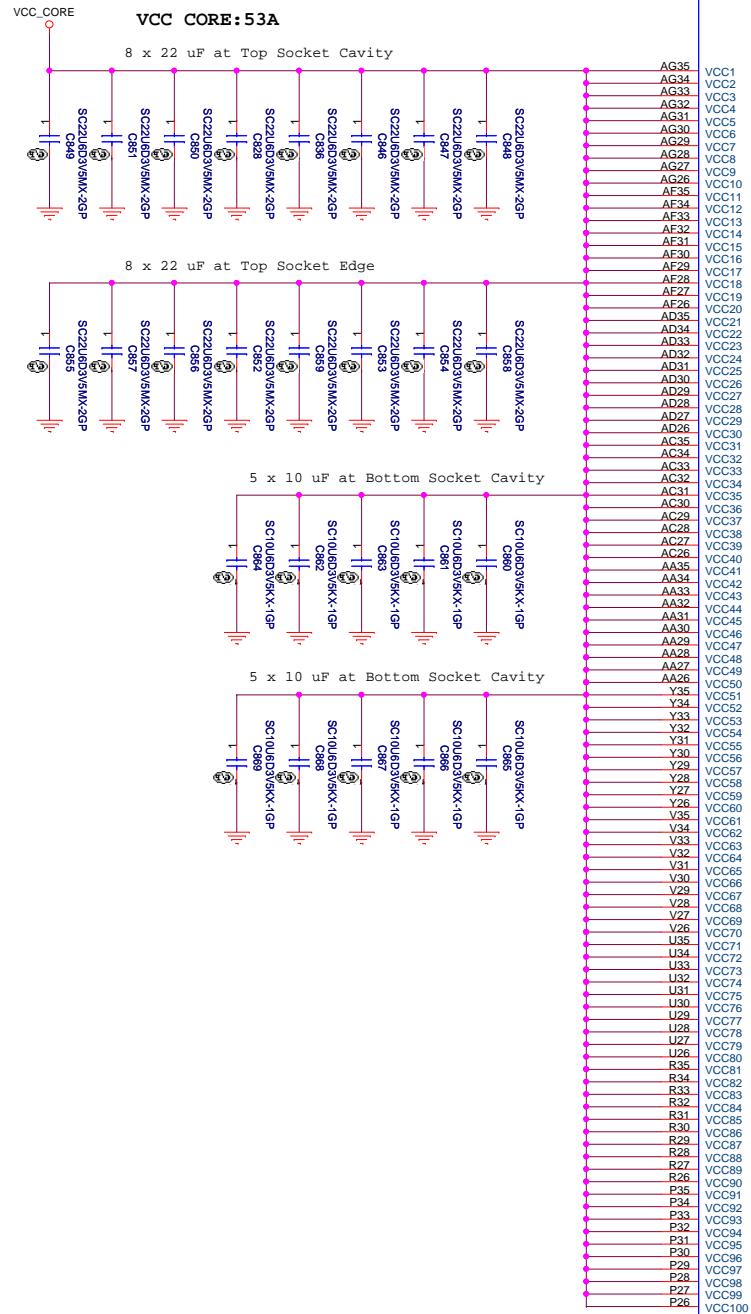


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CPU (RESERVED)		
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POWER



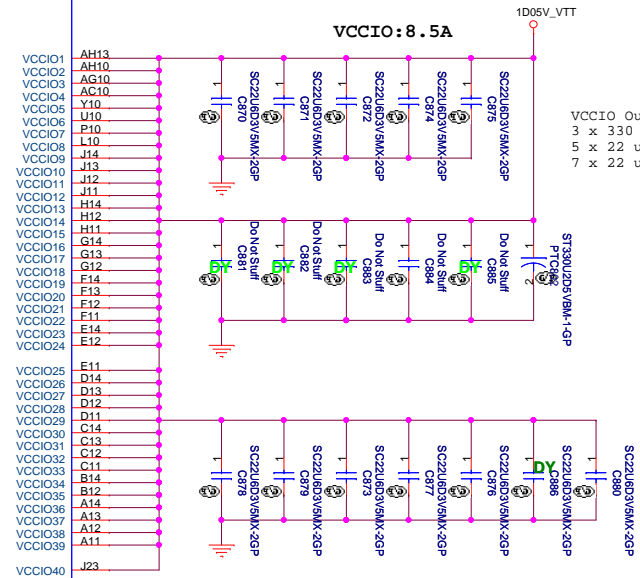
PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

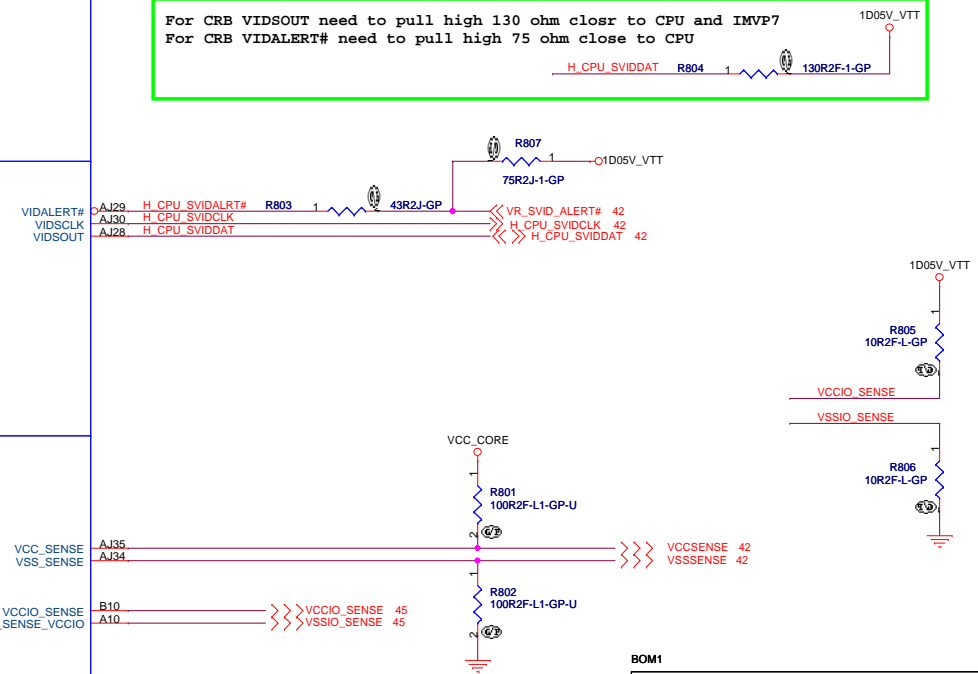
AUBURNF,CLARKUNF



VCCIO Output Decoupling Recommendation:

- 3 x 330 uF, 6mΩ
- 5 x 22 uF & 5 x 0805(no-stuff) MB Bottom Socket Cavity
- 7 x 22 uF & 2 x 0805(no-stuff) MB Top Socket Catity

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



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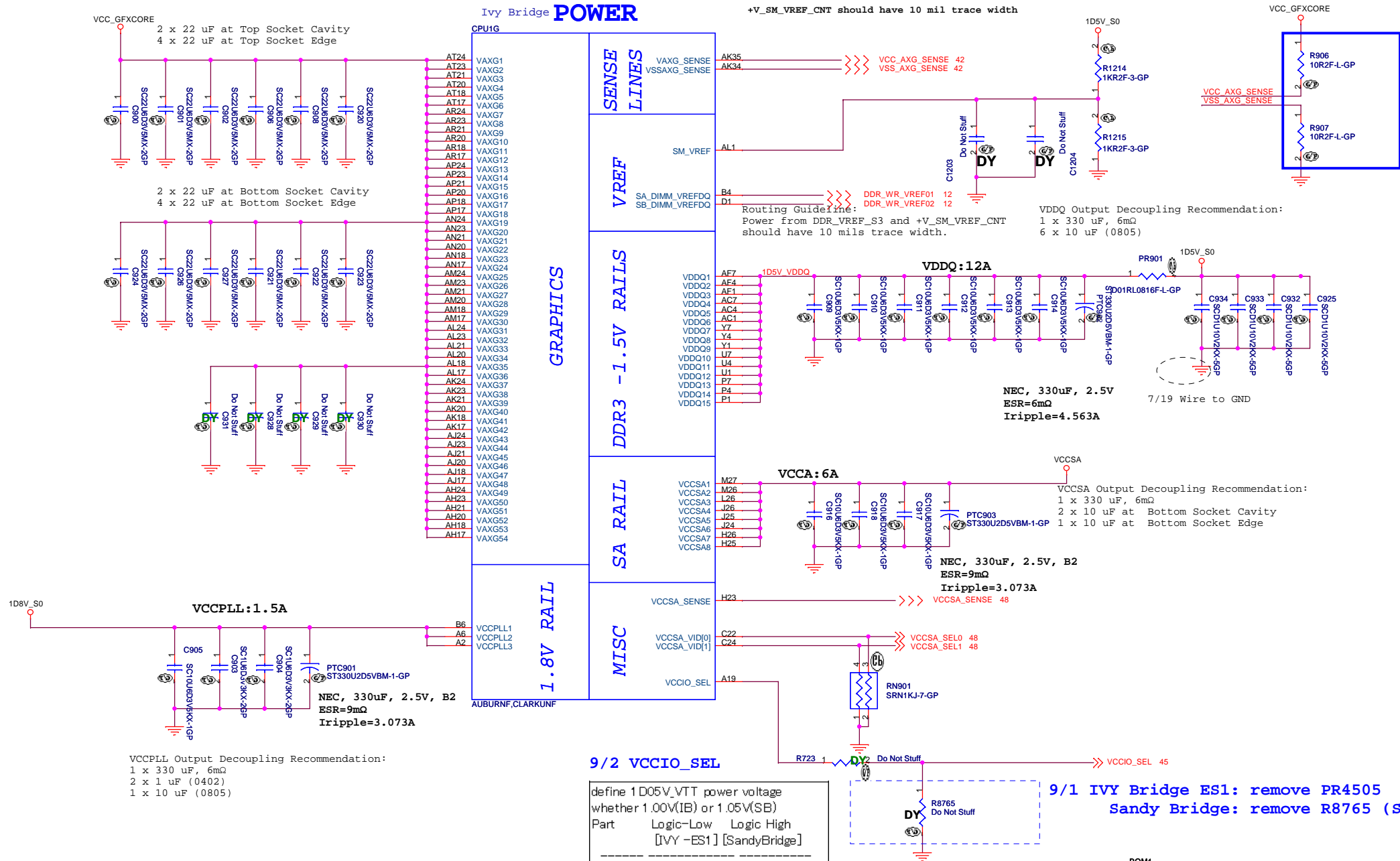
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Title			
CPU (VCC CORE)			
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Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

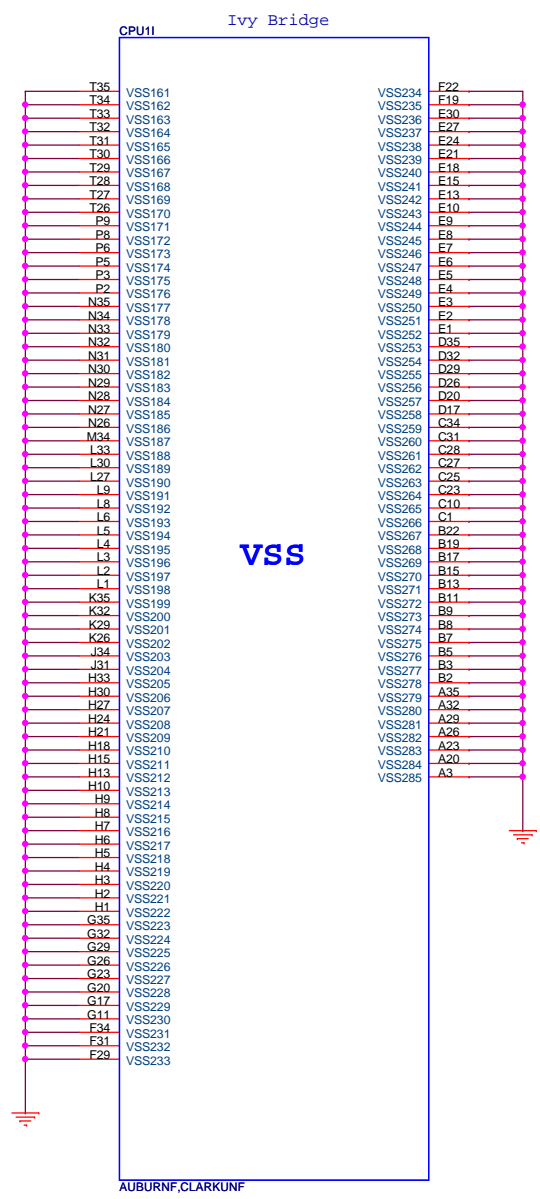
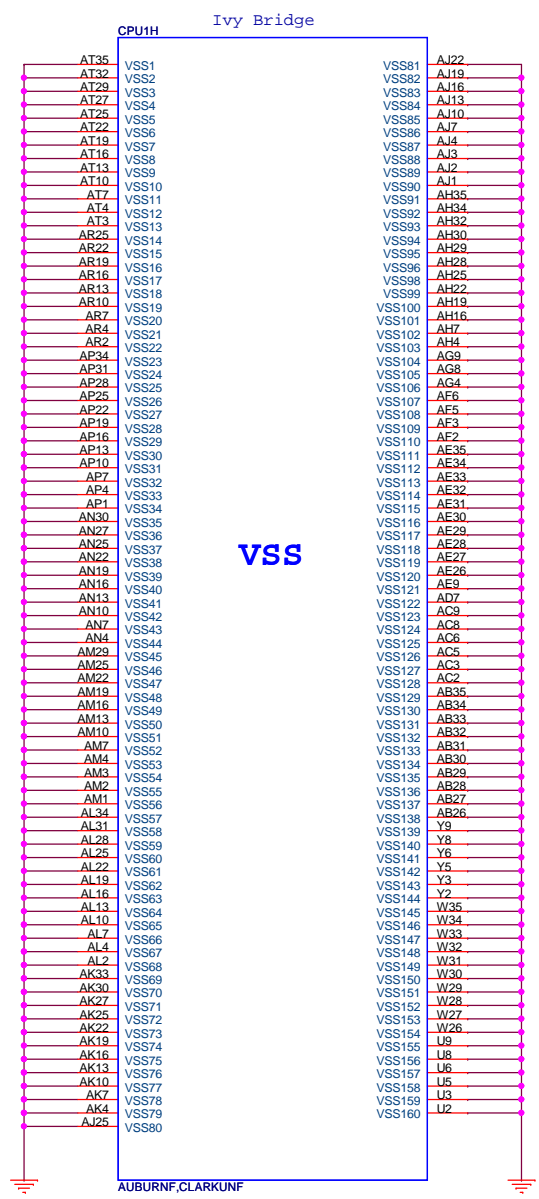
11/28 Wistron ORB change to 100ohm (64.10005.6DL), need verify

+V_SM_VREF_CNT should have 10 mil trace width



define 1D05V_VTT power voltage		
whether 1.00V(IB) or 1.05V(SB)		
Part	Logic-Low	Logic High
	[IVY-ES1]	[SandyBridge]
PR4505	DY	ASM
PR4525	(DY)	DY
PR4511	(DY)	DY
PR4518	ASM	ASM
R8765	ASM	DY

SSID = CPU



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File			
Size		CPU (VSS)	
A3		CD1 DIS	
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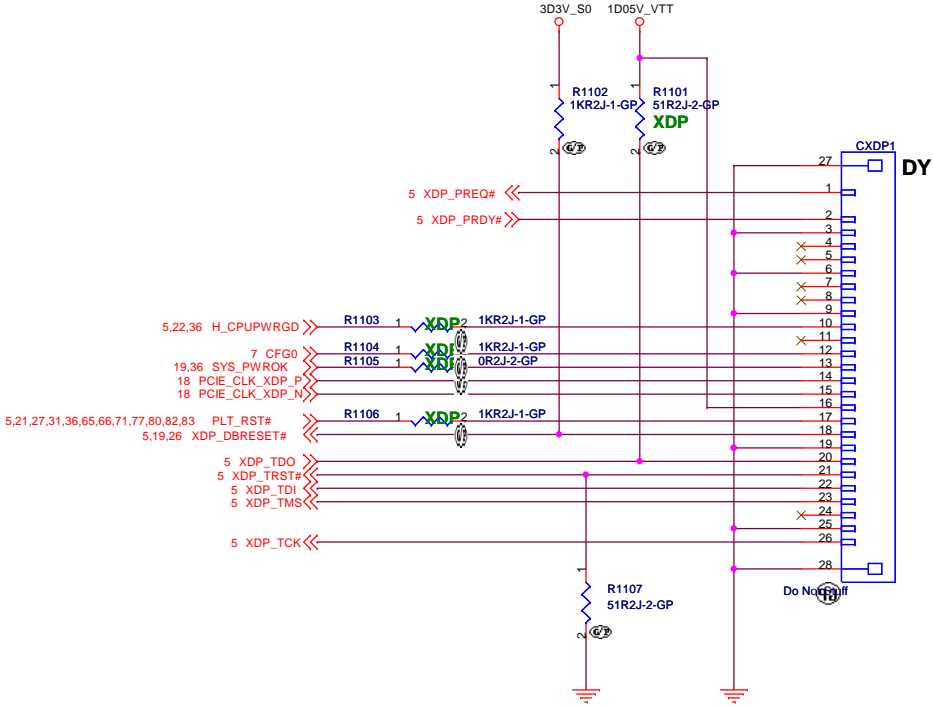
In production, All of parts should be not moounted except of pulldown 51 ohm on TRSTn and Pullup DBR#.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R1101	ASM	NOASM
TRST#	R1107	ASM	ASM
DBRESET#	R1102	ASM	ASM
PLT_RST#	R1106	ASM	NOASM
CFG0	R1104	ASM	NOASM
CPUPWRGD	R1103	ASM	NOASM
SYS_PWROK	R1105	ASM	NOASM
	CXDP1	ASM	NOASM

↑
LOGIC

9/2 CPU_XDP

Part	Enable	Disable
R1101	ASM	DY
R1107	ASM	ASM
R1102	ASM	ASM
R1106	ASM	DY
R1104	ASM	DY
R1103	ASM	DY
R1105	ASM	DY
CXDP1	ASM	DY

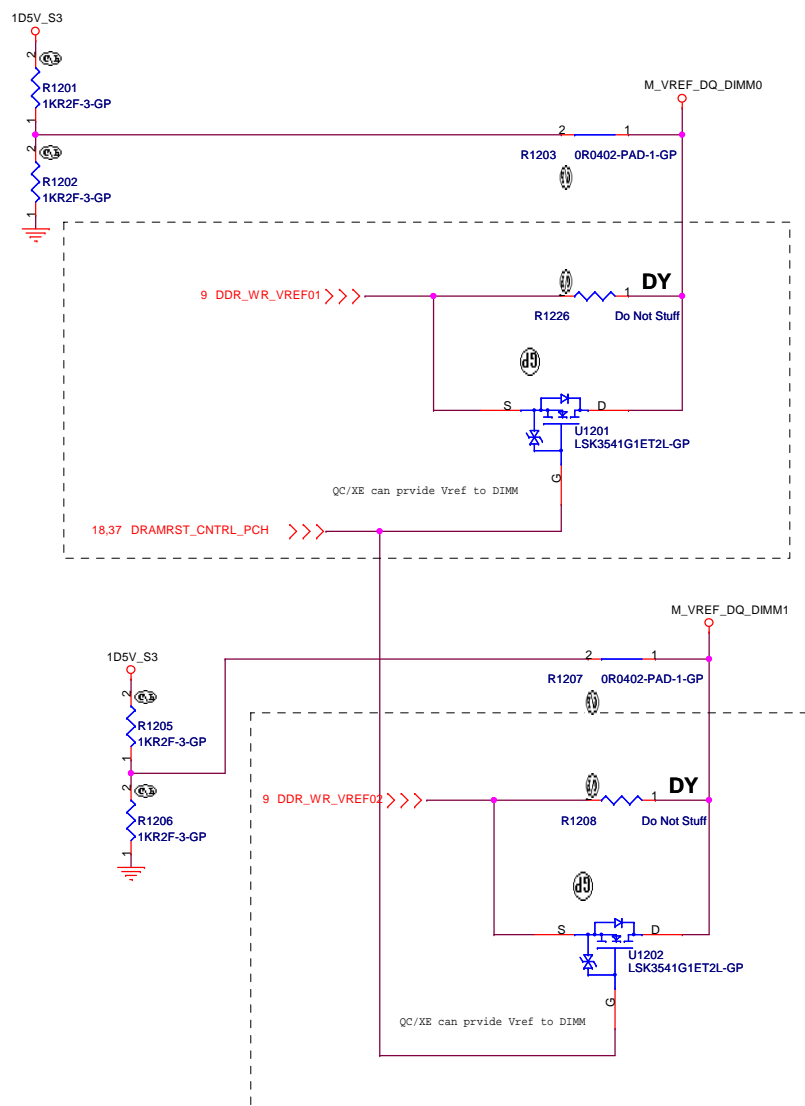


CPU_XDP_SFF_26pin_IF
Pin 1 OBSFN_A0 (PREQ#, I/O)
Pin 2 OBSFN_A1 (PRDY#, I/O)
Pin 3 GND
Pin 4 OBSFN_A0 (Open, I/O)
Pin 5 OBSFN_A1 (Open, I/O)
Pin 6 GND
Pin 7 OBSFN_A2 (Open, I/O)
Pin 8 OBSFN_A3 (Open, I/O)
Pin 9 GND
Pin 10 HOOK0 (PWRGD, In)
Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
Pin 12 HOOK2 (CFG0, Out)
Pin 13 HOOK3 (vr_READYSYS_PWROK, Out)
Pin 14 HOOK4 (BCLK#, In)
Pin 15 HOOK5 (BCLK#, In)
Pin 16 VCCOBS_AB (VCCP Voltage of CPU, In)
Pin 17 HOOK6 (RESET#, Out)
Pin 18 HOOK7 (DBR#, Out)
Pin 19 GND
Pin 20 TDO, In
Pin 21 TRST#, Out
Pin 22 TDI, Out
Pin 23 TMS, Out
Pin 24 TCK1 (Open)
Pin 25 GND
Pin 26 TCK0, Out

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VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation



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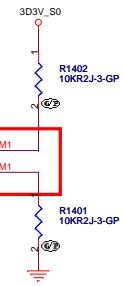
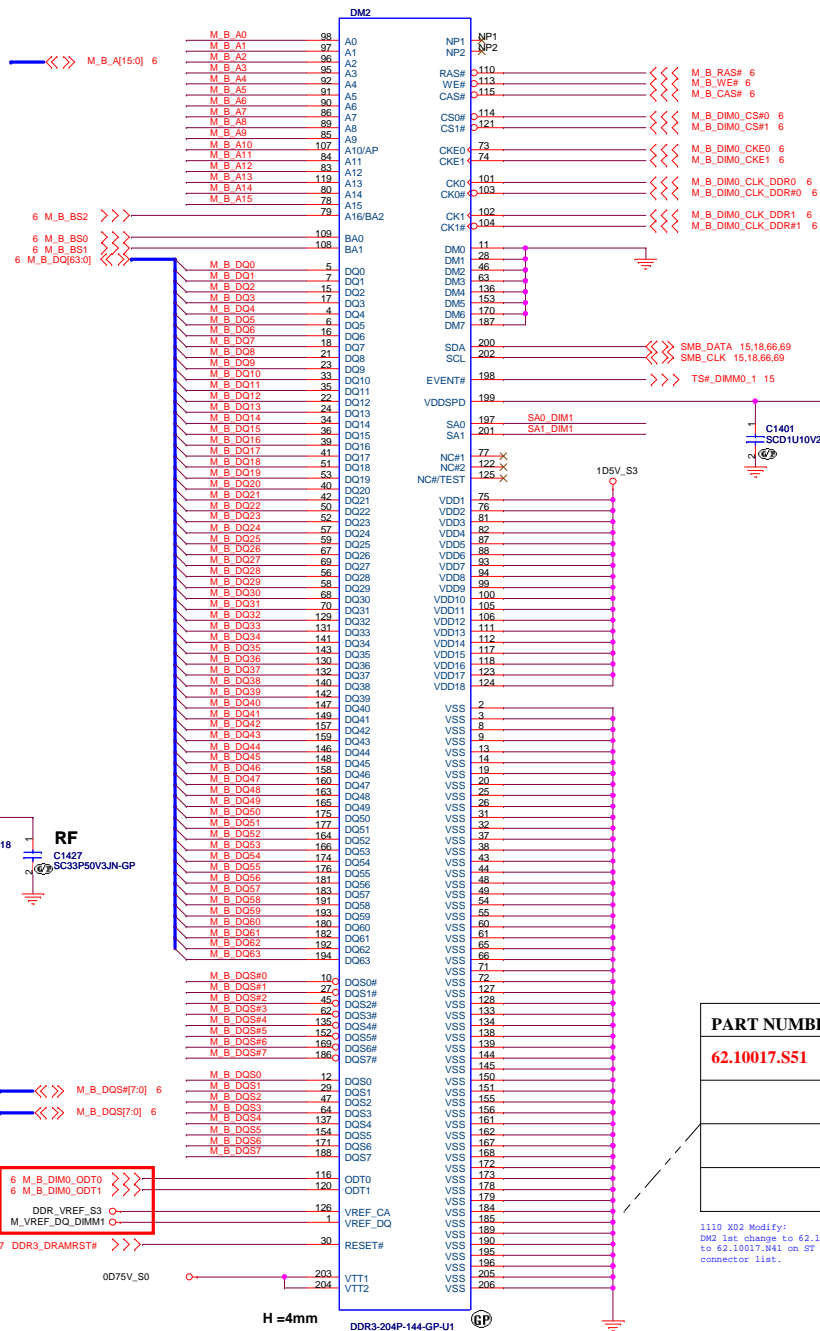
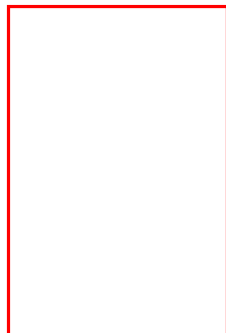
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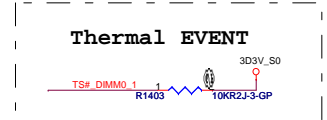
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20101231

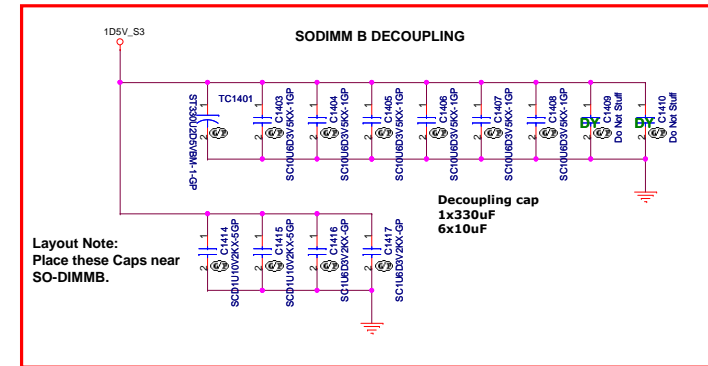


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from
the Processor than SO-DIMMA

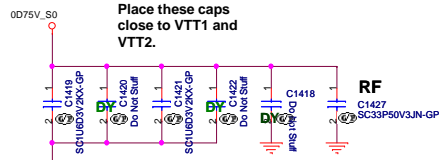


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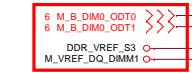
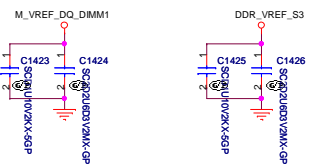


Layout Note:
Place these Caps near
SO-DIMMB.

Decoupling cap
1x330uF
6x10uF



Place these caps
close to VTT1 and
VTT2.



PART NUMBER	Height	TYPE
62.10017.S51	4mm	REVERSED
		REVERSED
		REVERSED
		REVERSED

1110 X02 Modify:
DM2 1st change to 62.10017.P41 2nd change
to 62.10017.P41 on ST stage from MS updated
connector list.

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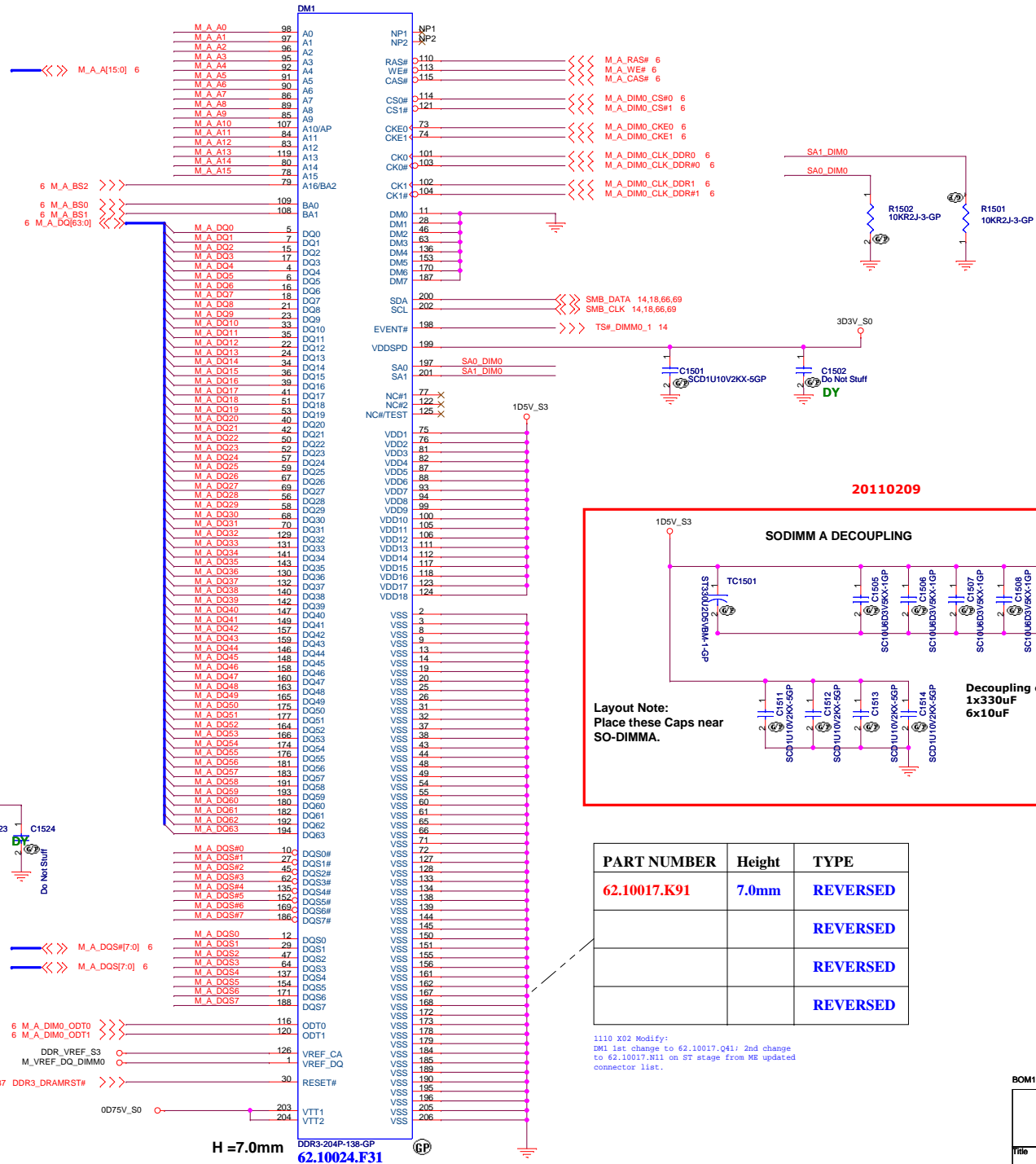
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Size Document Number **CD1 DIS** Rev **SC**

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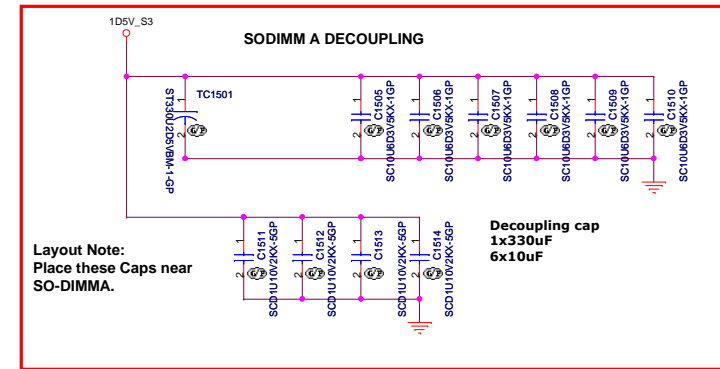
SSID = MEMORY

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Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2



PART NUMBER	Height	TYPE
62.10017.K91	7.0mm	REVERSED
		REVERSED
		REVERSED
		REVERSED

```

1110 X02 Modify:
DM1 list change to 62.10017.Q41; 2nd change
to 62.10017.N11 on ST stage from ME updated
connector list.

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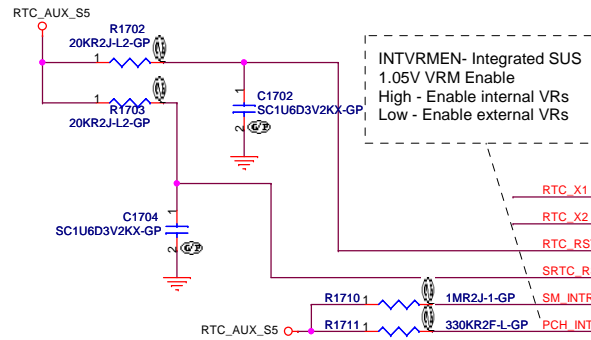
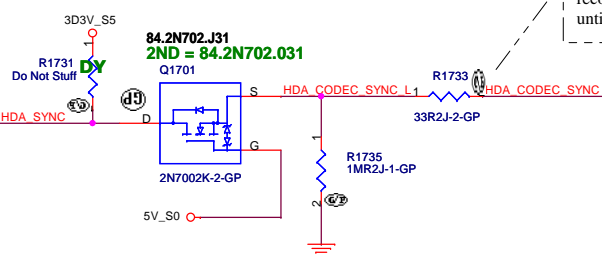
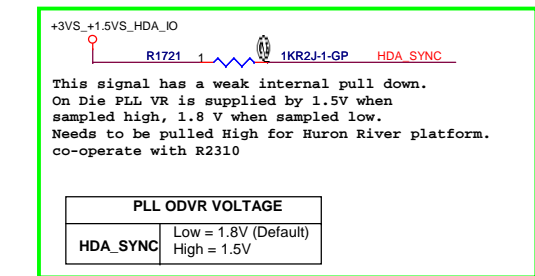
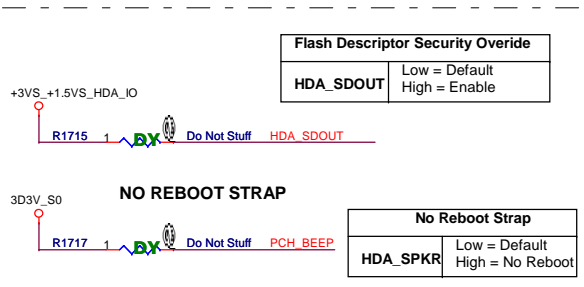
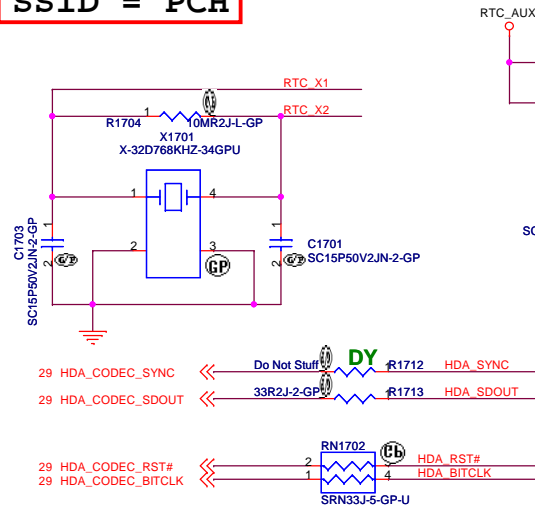
Title			
DDR3 SO-DIMM1			
Size	Document Number		Rev
Custom	CD1 DIS		SC
Date:	Tuesday, December 13, 2011	Sheet 15 of	102

(Blanking)

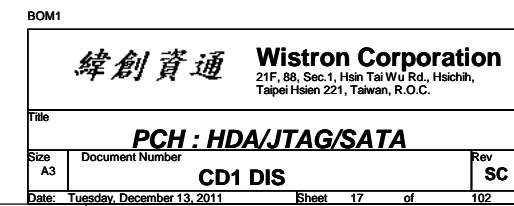
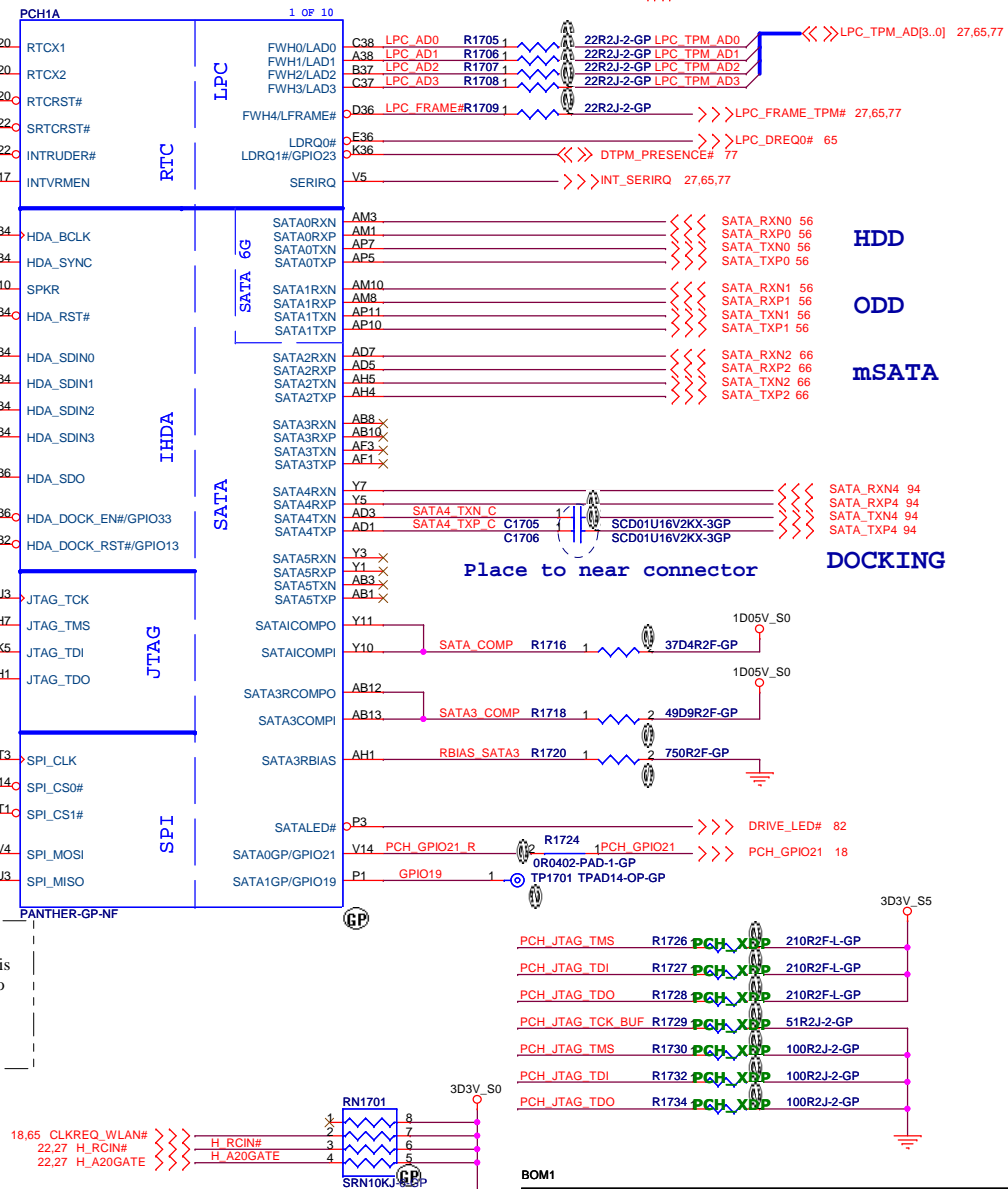
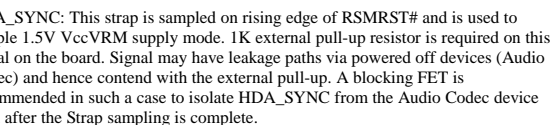
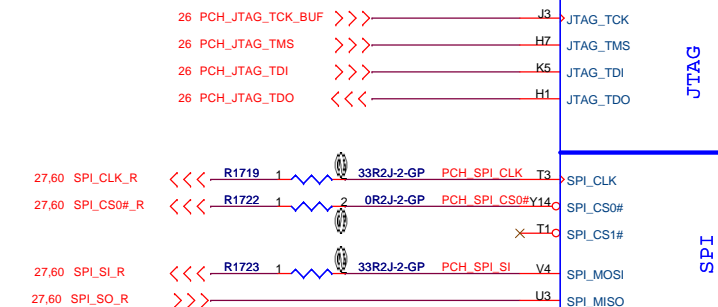
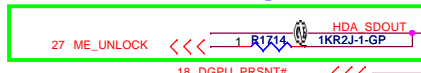
BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A3	CD1 DIS		SC
Date:	Tuesday, December 13, 2011	Sheet	16 of 102

SSID = PCH

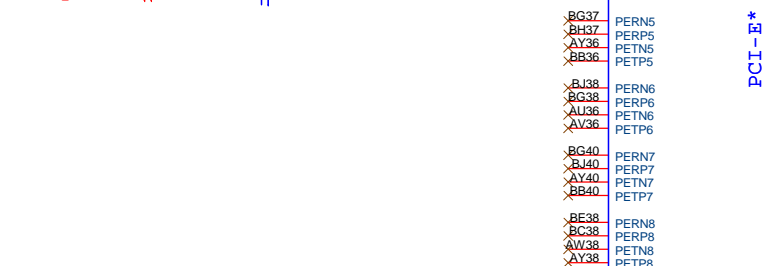
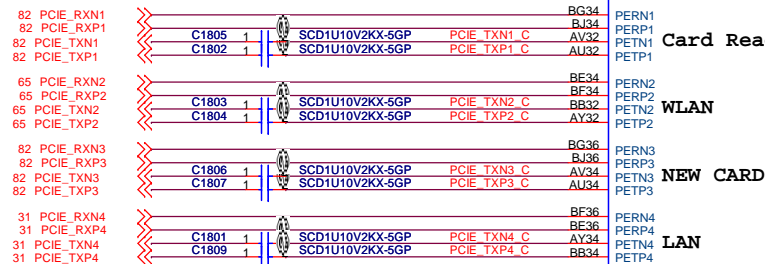


Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

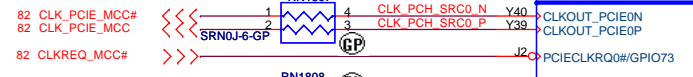


SSID = PCH

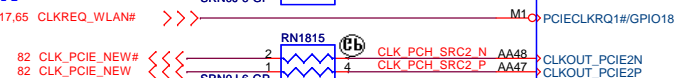
If PCIE port 1 is disabled, it will cause all PCIE port disabled



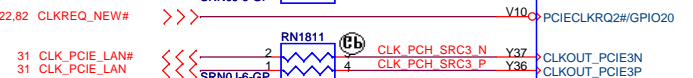
Card Reader CLK



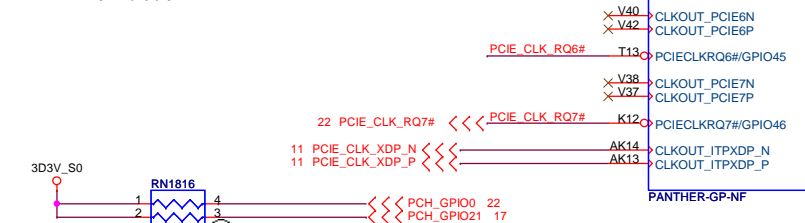
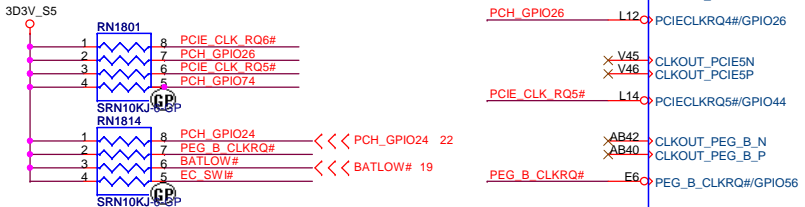
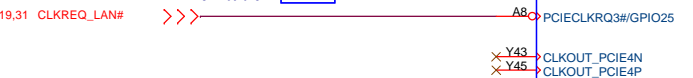
WLAN CLK 65 CLK_PCIE_WLAN# <
65 CLK_PCIE_WLAN >



EXC CLK



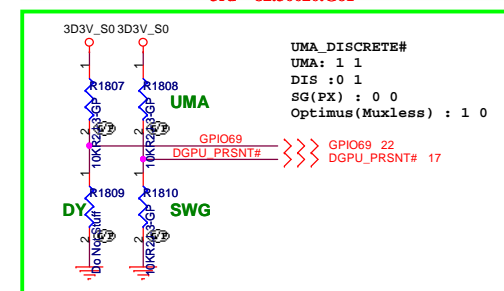
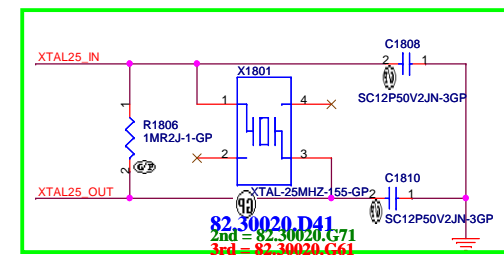
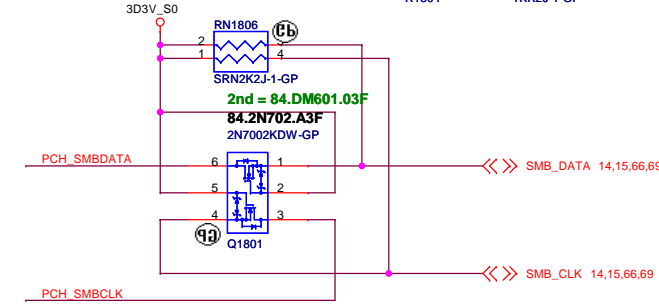
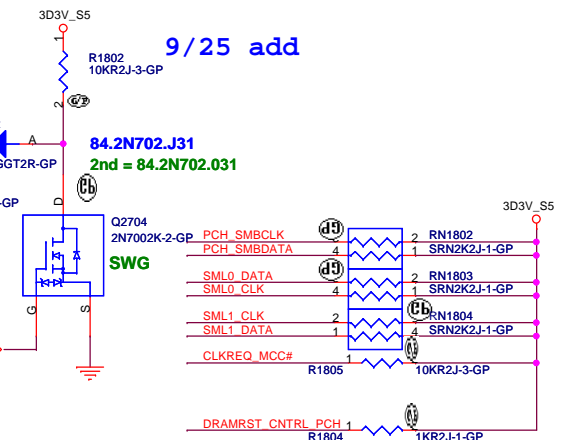
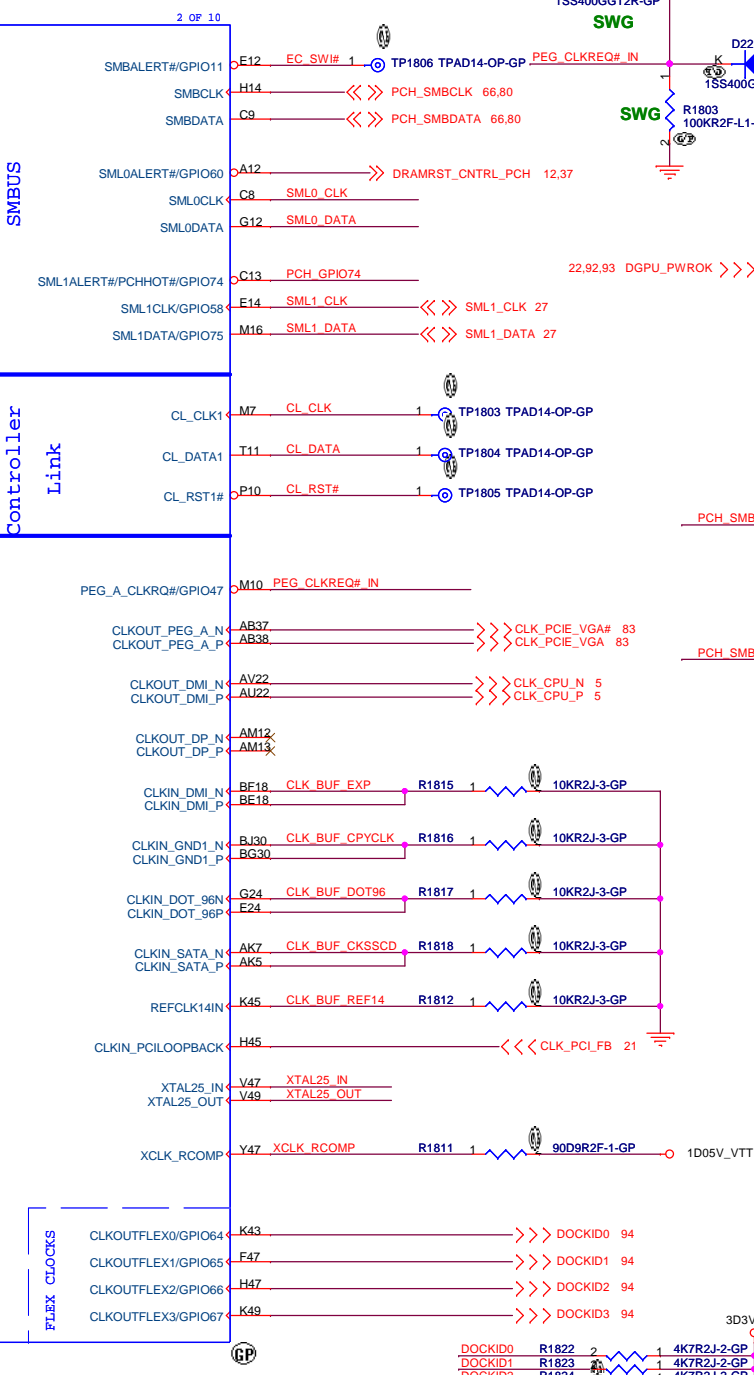
LAN CLK



PCIECLKRQ1# and PCIECLKRQ2#

Support 80 power only

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

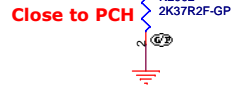
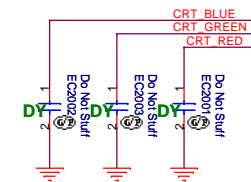
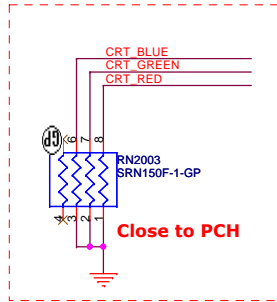
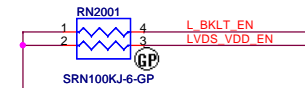
Title			
PCH : PCIE/SMBUS/CLK			
Size A3	Document Number		Rev S0
	CD1 DIS		
Date:	Tuesday, December 13, 2011	Sheet 18 of	102

SSID = PCH

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30



L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display



27 L_BKLT_EN
49 LVDS_VDD_EN
49 L_BKLT_CTRL
49 LVDS_DDC_CLK
49 LVDS_DDC_DATA

TPAD14-OP-GP TP2001

49 LVDSA_CLK#
49 LVDSA_CLK
49 LVDSA_DATA0#
49 LVDSA_DATA1#
49 LVDSA_DATA2#

49 LVDSA_DATA0
49 LVDSA_DATA1
49 LVDSA_DATA2

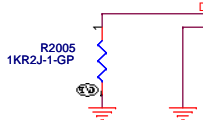
49 LVDSB_CLK#
49 LVDSB_CLK
49 LVDSB_DATA0#
49 LVDSB_DATA1#
49 LVDSB_DATA2#

49 LVDSB_DATA0
49 LVDSB_DATA1
49 LVDSB_DATA2

50 CRT_BLUE
50 CRT_GREEN
50 CRT_RED

50 CRT_DDC_CLK
50 CRT_DDC_DATA

50 CRT_HSYNC
50 CRT_VSYNC



PCH1D

L_BKLTEN
L_VDD_EN

L_BKLTCTL
L_DDC_CLK
L_DDC_DATA

L_CTRL_CLK
L_CTRL_DATA

LVD_IBG
LVD_VBG

LVD_VREFH
LVD_VREFL

LVDSA_CLK#
LVDSA_CLK

LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3

LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3

LVDSB_CLK#
LVDSB_CLK

LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3

LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3

CRT_BLUE
CRT_GREEN
CRT_RED

CRT_DDC_CLK
CRT_DDC_DATA

CRT_HSYNC
CRT_VSYNC

DAC_IREF_R
DAC_IRTN

PANTHER-GP-NF

LVDS

CRT

Digital Display Interface

SDVO_TVCLKINN
SDVO_TVCLKINP

SDVO_STALLN
SDVO_STALLP

SDVO_INTN
SDVO_INTP

SDVO_CTRLCLK
SDVO_CTRLDATA

DDPB_AUXN
DDPB_AUXP
DDPB_HPD

DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P

DDPC_CTRLCLK
DDPC_CTRLDATA

DDPC_AUXN
DDPC_AUXP
DDPC_HPD

DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P

DDPD_CTRLCLK
DDPD_CTRLDATA

DDPD_AUXN
DDPD_AUXP
DDPD_HPD

DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P

DPD_LANE0N
DPD_LANE0P
DPD_LANE1N
DPD_LANE1P
DPD_LANE2N
DPD_LANE2P
DPD_LANE3N
DPD_LANE3P

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DPD_LANE3P

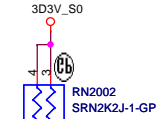
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DPD_LANE3P

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DPD_LANE3P

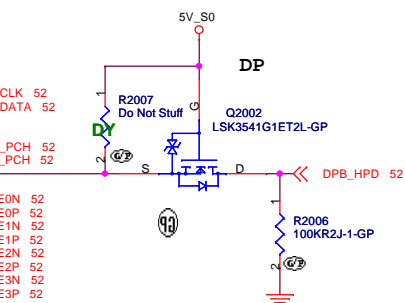
DPD_LANE0N
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DPD_LANE2P
DPD_LANE3N
DPD_LANE3P

DPD_LANE0N
DPD_LANE0P
DPD_LANE1N
DPD_LANE1P
DPD_LANE2N
DPD_LANE2P
DPD_LANE3N
DPD_LANE3P



DDI Port B Detect:(SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected



PORT	DDI PCH Pin Names	SDVO Mapping	DisplayPort Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

BOM1

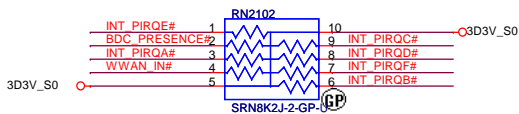
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : LVDS/CRT/DDI**

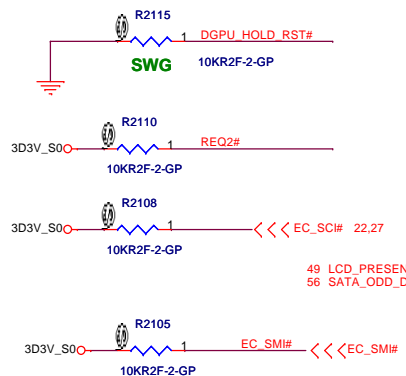
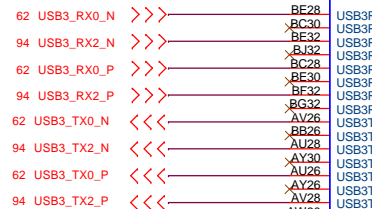
Size A3 Document Number: **CD1 DIS** Rev: **SC**

Date: Tuesday, December 13, 2011 Sheet 20 of 102

SSID = PCH



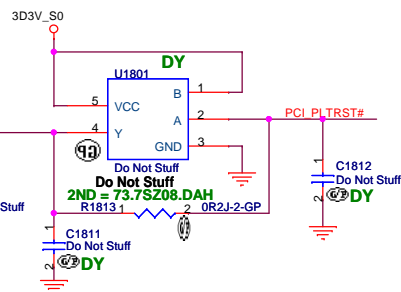
For PPT USB3.0 feature



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

GPIO51 and GPIO19 Internal PU

5,11,27,31,36,65,66,71,77,80,82,83 PLT_RST#



RSVD

PCI

USB

PCH1E

5 OF 10

TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20

TP21
TP22
TP23
TP24

INT_PIRQA# K40C
INT_PIRQB# K38C
INT_PIRQC# H38C
INT_PIRQD# G38C

REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54

G42C
G40C
G44C
G46C

INT_PIRQA# K40C
INT_PIRQB# K38C
INT_PIRQC# H38C
INT_PIRQD# G38C

REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54

G42C
G40C
G44C
G46C

INT_PIRQA# K40C
INT_PIRQB# K38C
INT_PIRQC# H38C
INT_PIRQD# G38C

REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54

G42C
G40C
G44C
G46C

INT_PIRQA# K40C
INT_PIRQB# K38C
INT_PIRQC# H38C
INT_PIRQD# G38C

REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54

G42C
G40C
G44C
G46C

INT_PIRQA# K40C
INT_PIRQB# K38C
INT_PIRQC# H38C
INT_PIRQD# G38C

REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54

G42C
G40C
G44C
G46C

RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
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USBP0N
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USBP13P

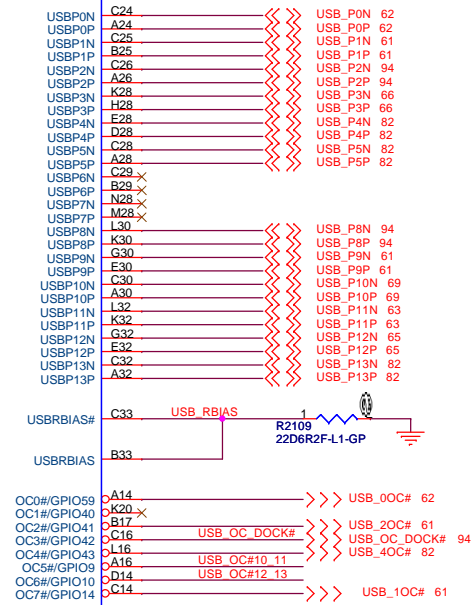
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USBP1N
USBP1P
USBP2N
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USBP4P
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USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
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USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P

USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
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USBP9N
USBP9P
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USBP11P
USBP12N
USBP12P
USBP13N
USBP13P

Utilize Port 9 for USB debug



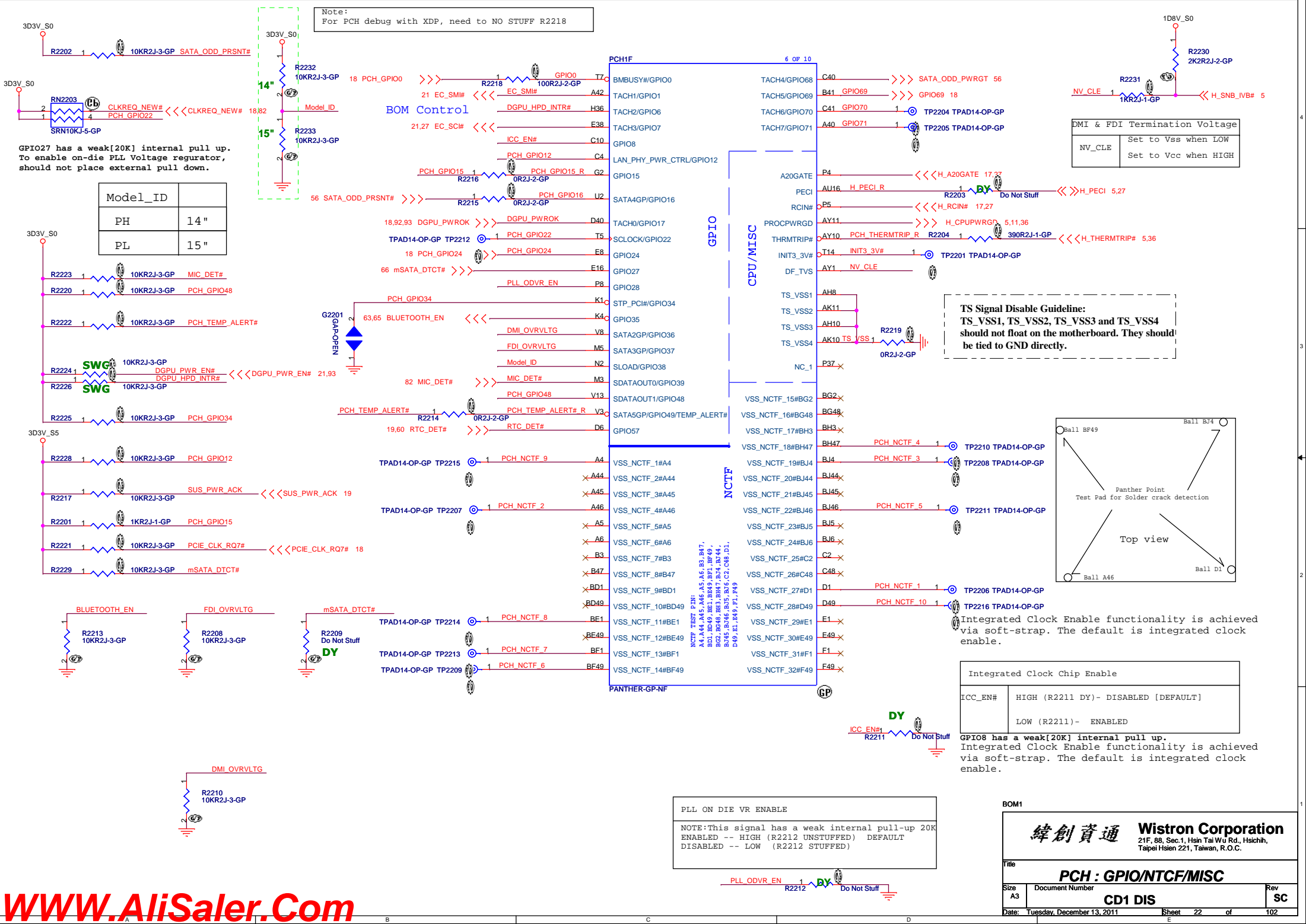
OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB Table

Pair	Device
0	USB3.0 port 0
1	USB2.0 port 1
2	USB3.0 Docking
3	WWAN
4	USB2.0 port (AUO4)
5	New Card
6	X
7	X
8	USB2.0 Docking
9	USB2.0 port 2
10	FPR
11	BLUETOOTH
12	WLAN
13	Camera

BOM1

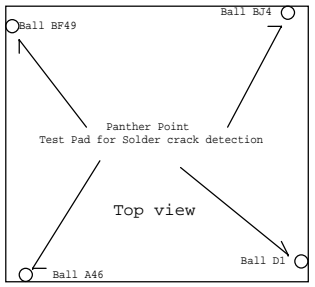
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.



Note:
For PCH debug with XDP, need to NO STUFF R2218

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW
NV_CLE	Set to Vcc when HIGH

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4
should not float on the motherboard. They should
be tied to GND directly.



Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
ICC_EN#	LOW (R2211)- ENABLED

PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

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Title

PCH : GPIO/NTCF/MISC

Size

A3

Document Number

CD1 DIS

Date

Tuesday, December 13, 2011

Sheet

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of

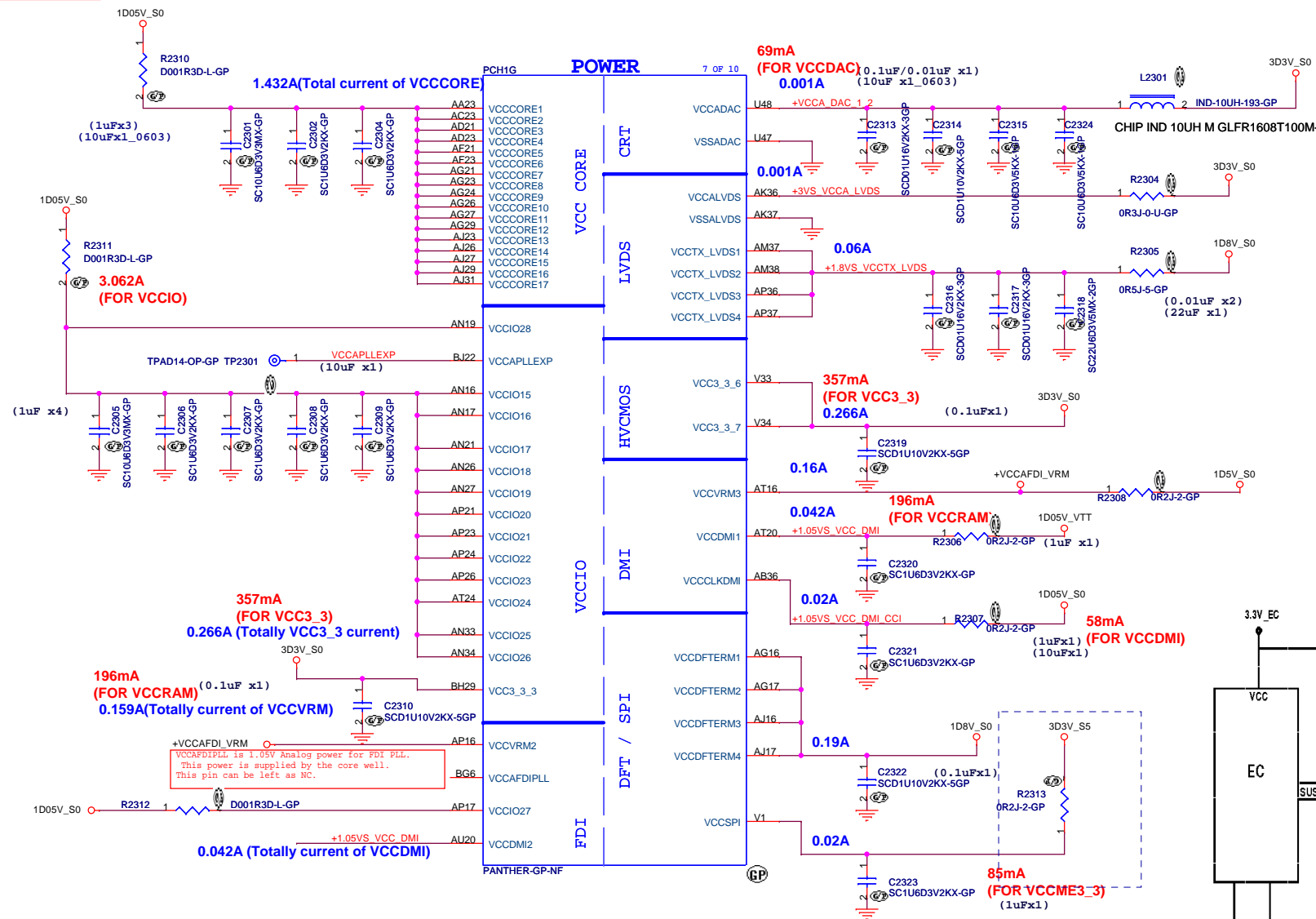
102

Rev

SC

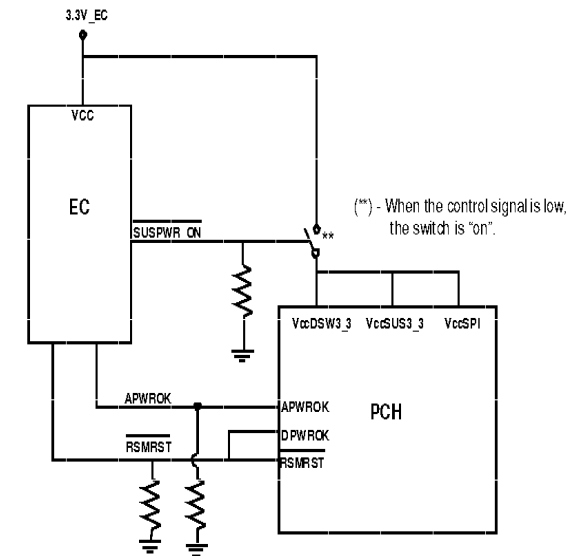
BOM1

SSID = PCH 6A

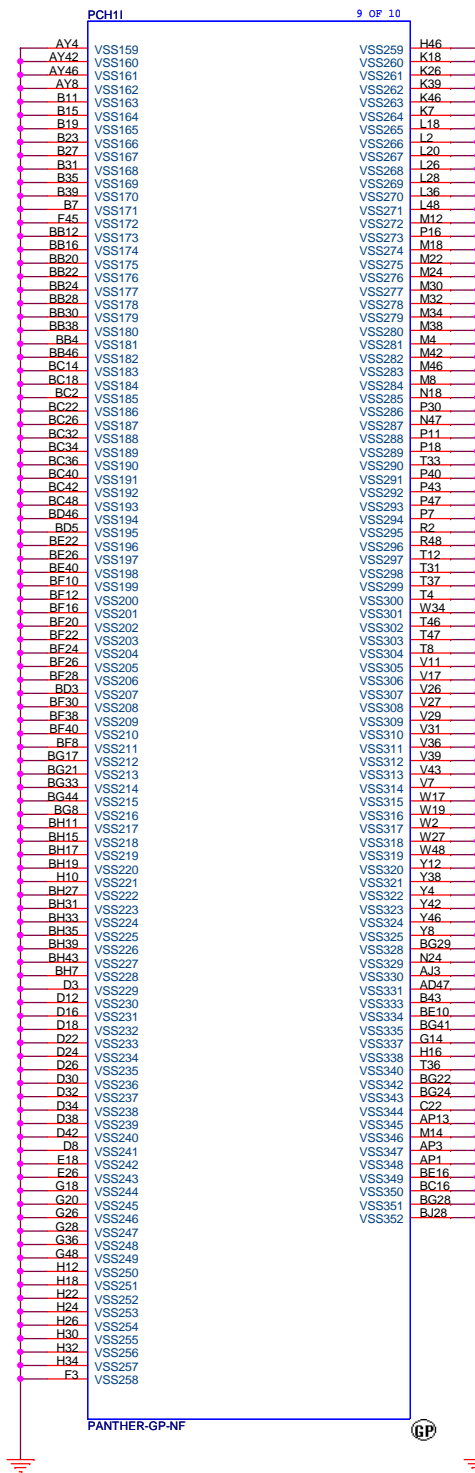
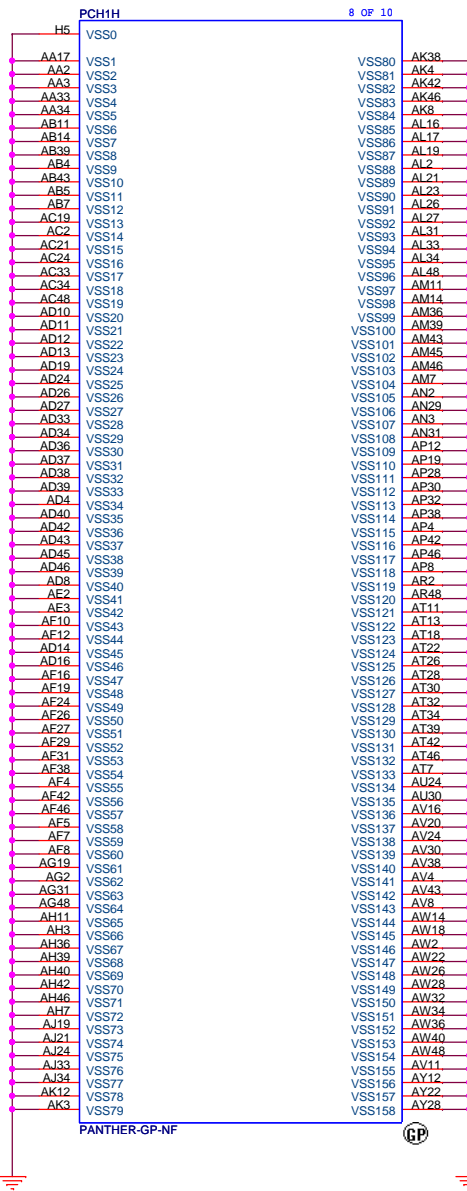


Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture



SSID = PCH



BOM1

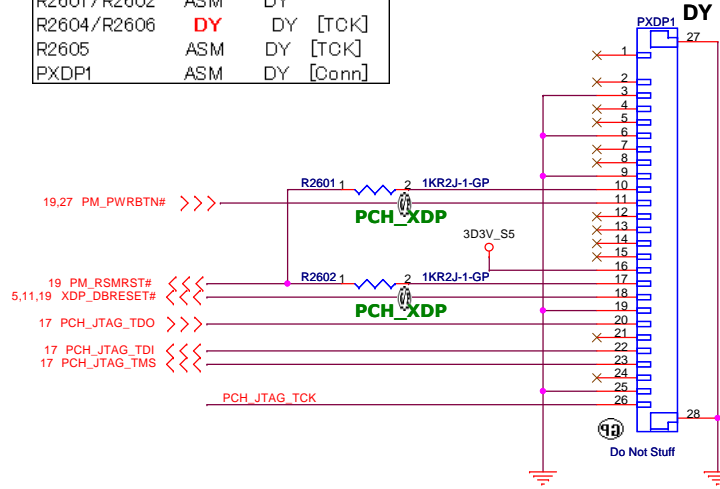
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			PCH : VSS	
Size	Document Number	Rev		SC
A3	CD1 DIS			
Date:	Tuesday, December 13, 2011	Sheet	25	of 102

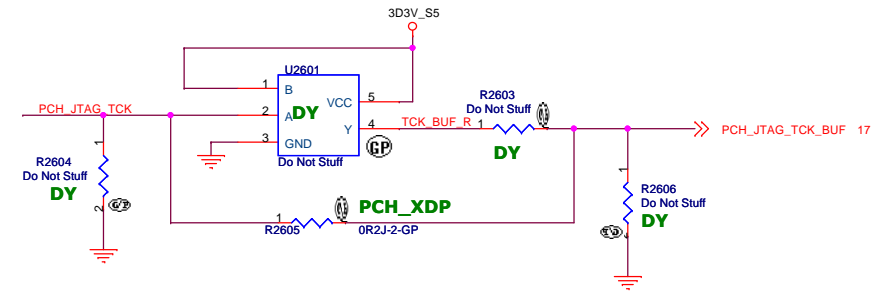
9/2 PCH_XDP

Part	Enable	Disable
R1726/R1730	ASM	ASM [TMS]
R1727/R1731	ASM	ASM [TDI]
R1728/R1732	ASM	DY [TDO]
R1729	ASM	DY [TCK]
R2601/R2602	ASM	DY
R2604/R2606	DY	DY [TCK]
R2605	ASM	DY [TCK]
PXDP1	ASM	DY [Conn]

PCH XDP



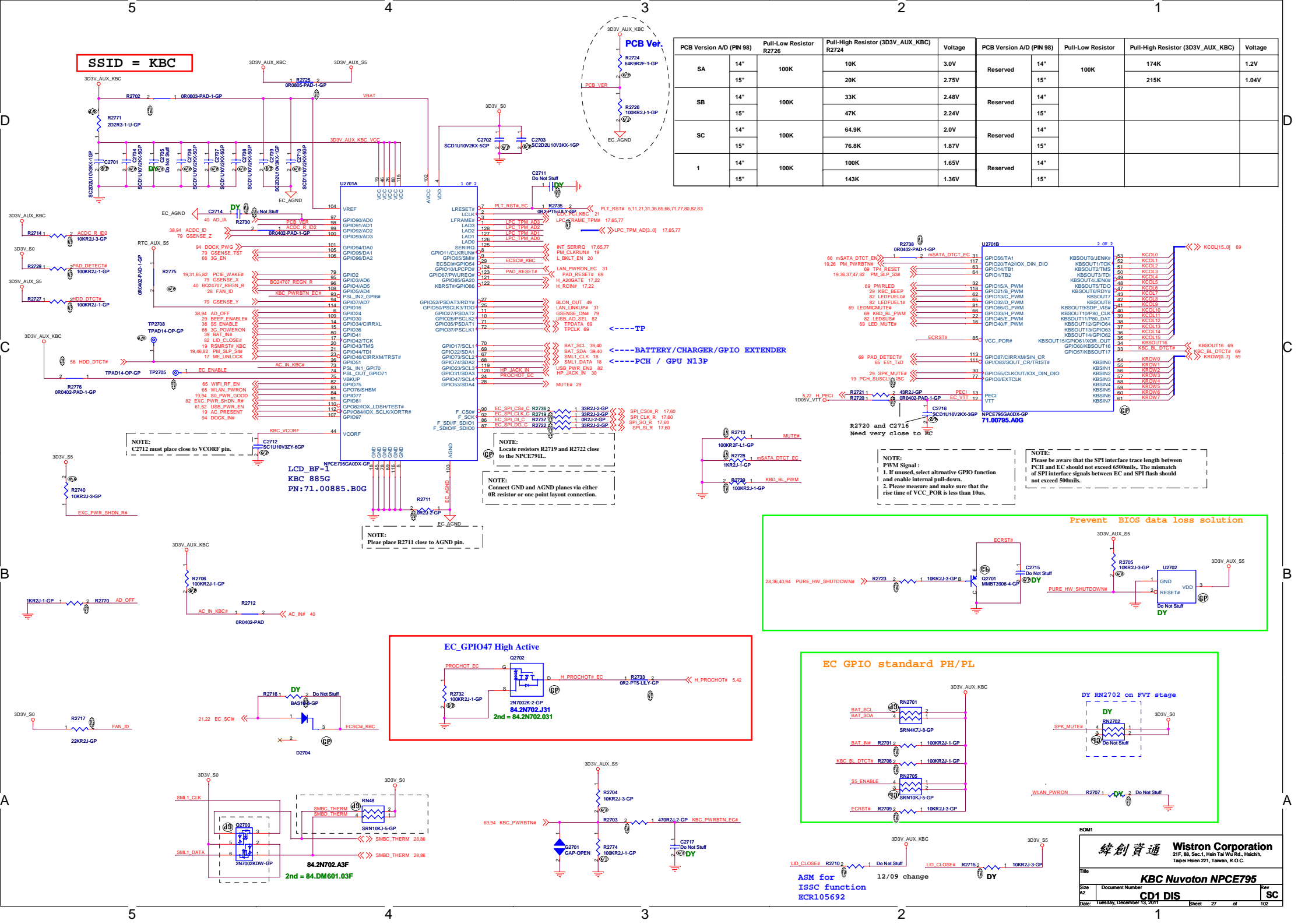
DY in SVT



BOM1

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Title			PCH XDP		
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A3	CD1 DIS				
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Thermal sensor



Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11

3D3V_S0



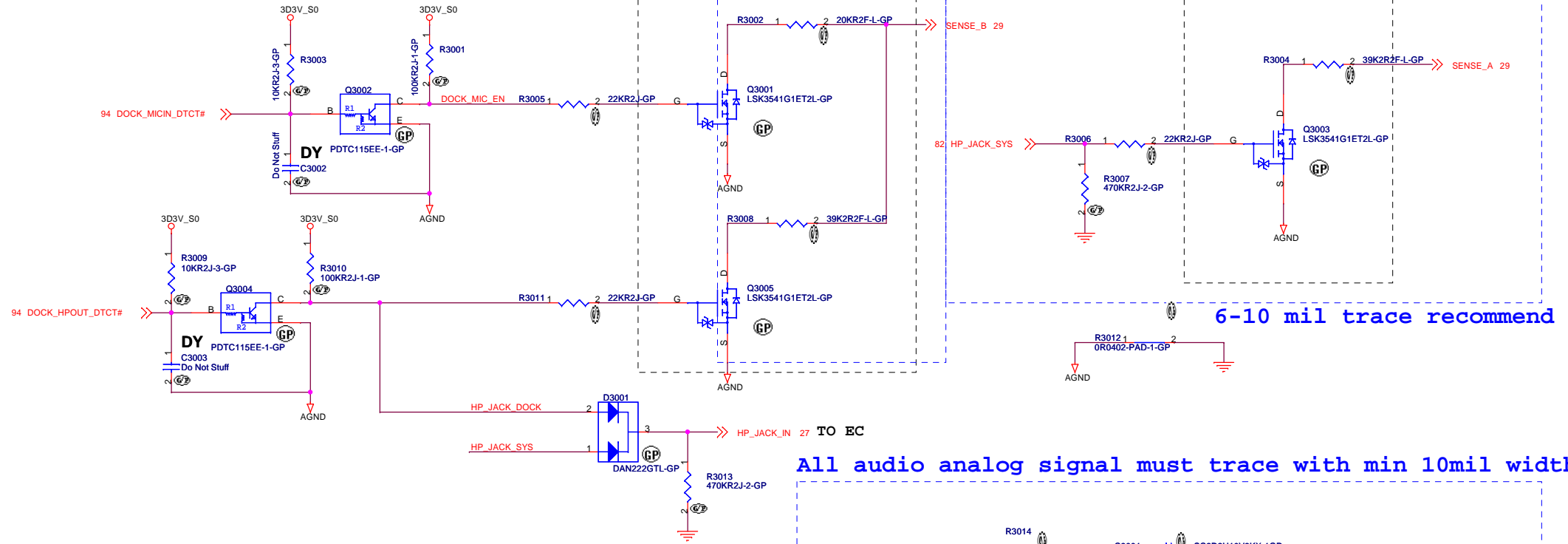
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Audio Codec ALC3202			
Size A2	Document Number		Rev
	CD1 DIS		SC
Date: Tuesday, December 13, 2011		Sheet 29	of 102

6-10 mil trace recommend

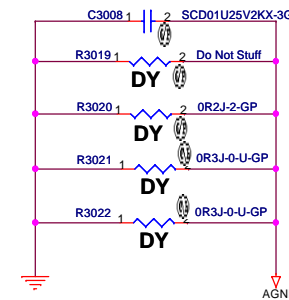
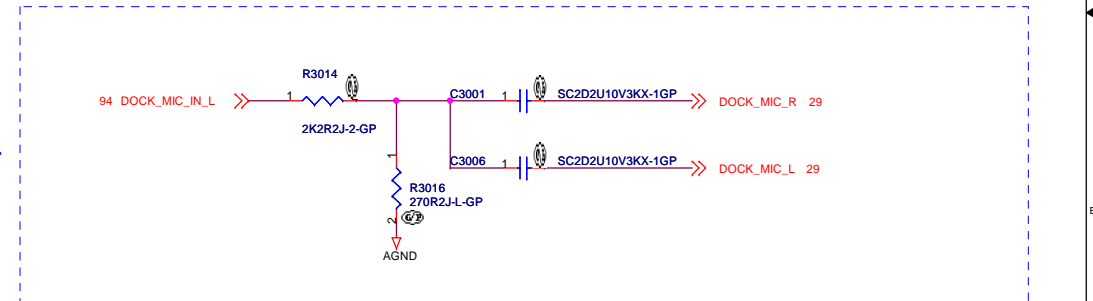
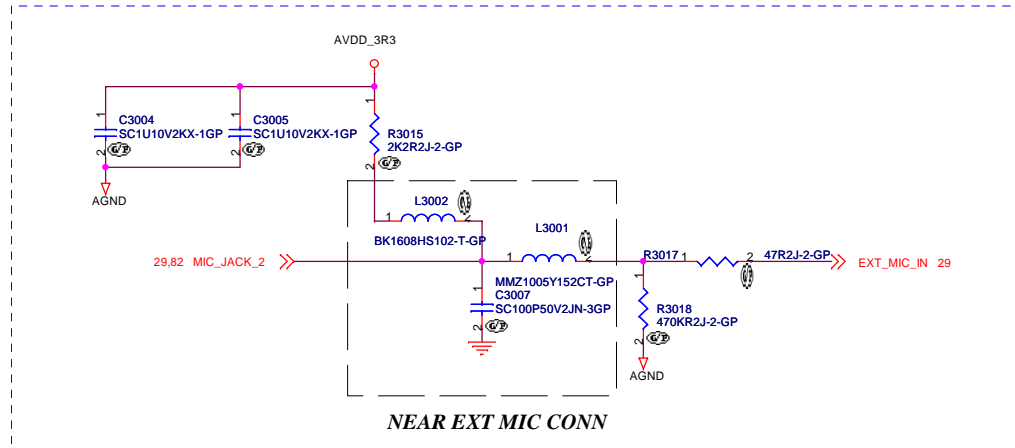
CLOSE TO CODEC

CLOSE TO CODEC



All audio analog signal must trace with min 10mil width

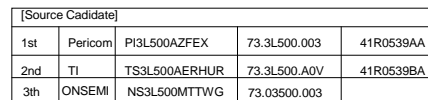
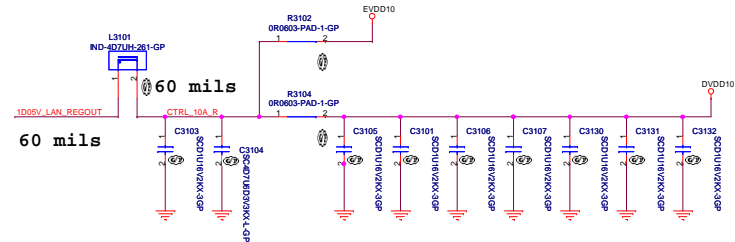
All audio analog signal must trace with min 10mil width



BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title			Speaker Conn	
Size	Document Number	CD1 DIS		Rev
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BOM1

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Title

Reserved

Reserved

Size
A3

Document Number
CD1 DIS

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SC

Date: Tuesday, December 13, 2011

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BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>	<div>Rev</div>	<div>SC</div>
<div>A3</div>	<div>CD1 DIS</div>	<div>102</div>	<div>33</div>
<div>Date: Tuesday, December 13, 2011</div>		<div>Sheet</div>	<div>of</div>
<div>1</div>		<div>33</div>	<div>102</div>

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BOM1

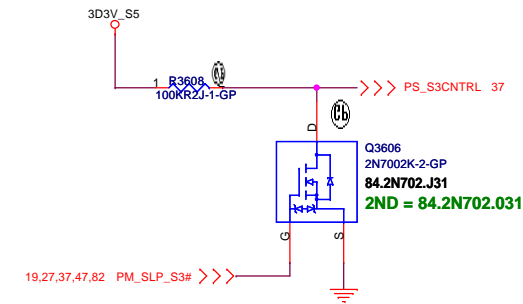
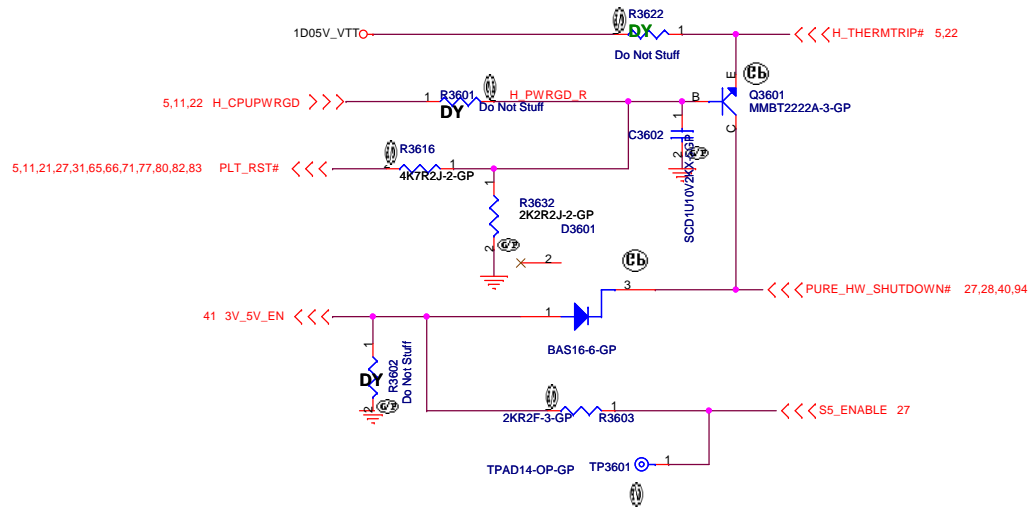
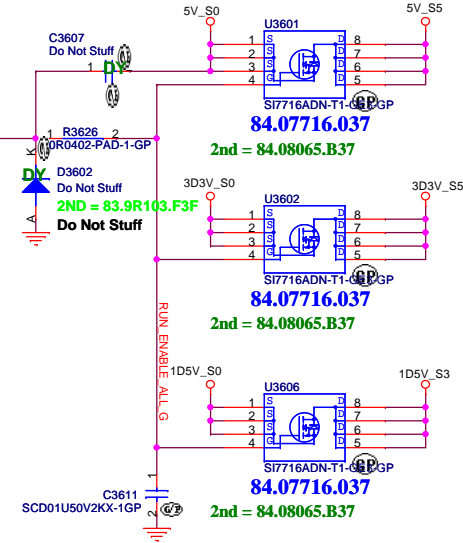
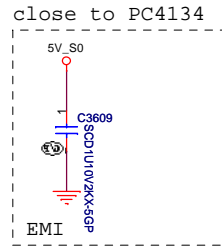
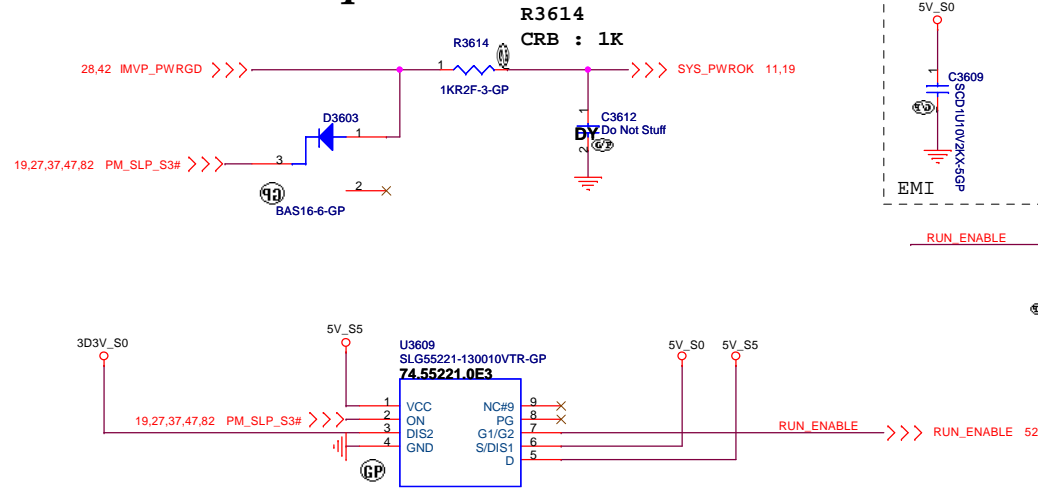
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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Size	Document Number	Rev	
A3	CD1 DIS	SC	
Date:	Tuesday, December 13, 2011	Sheet	34 of 102

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BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
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<div>Size</div>	<div>Document Number</div>	<div>Rev</div>	<div>SC</div>
<div>A3</div>	<div>CD1 DIS</div>	<div>102</div>	<div>35</div>
<div>Date: Tuesday, December 13, 2011</div>		<div>Sheet</div>	<div>of</div>
<div>1</div>		<div>35</div>	<div>102</div>

Power Sequence

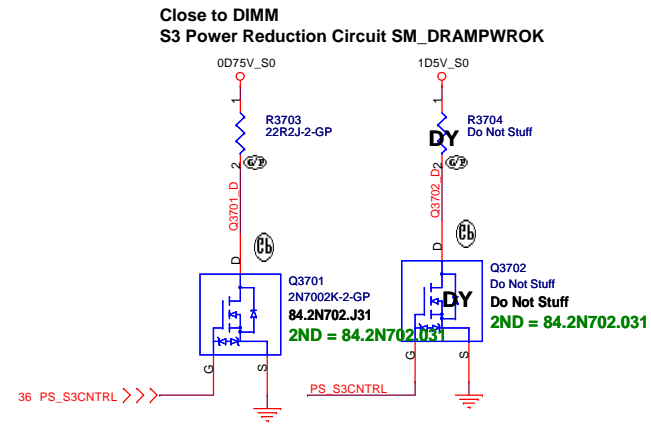
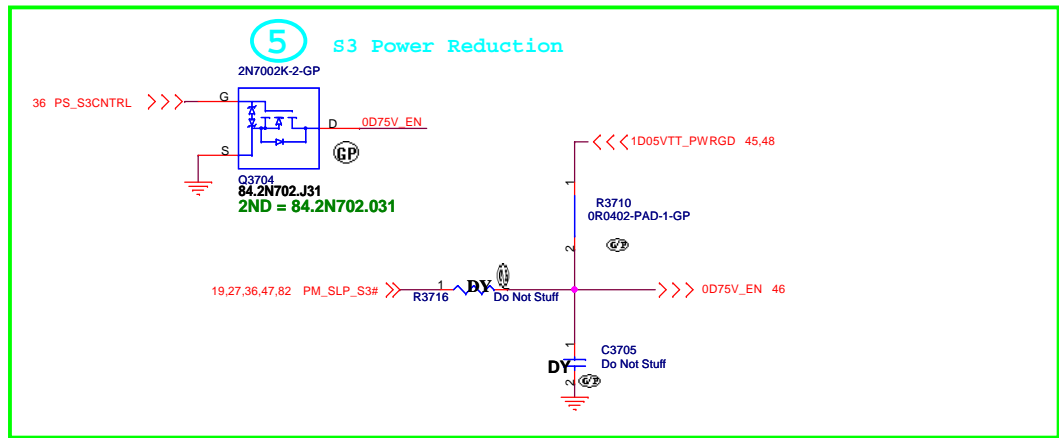
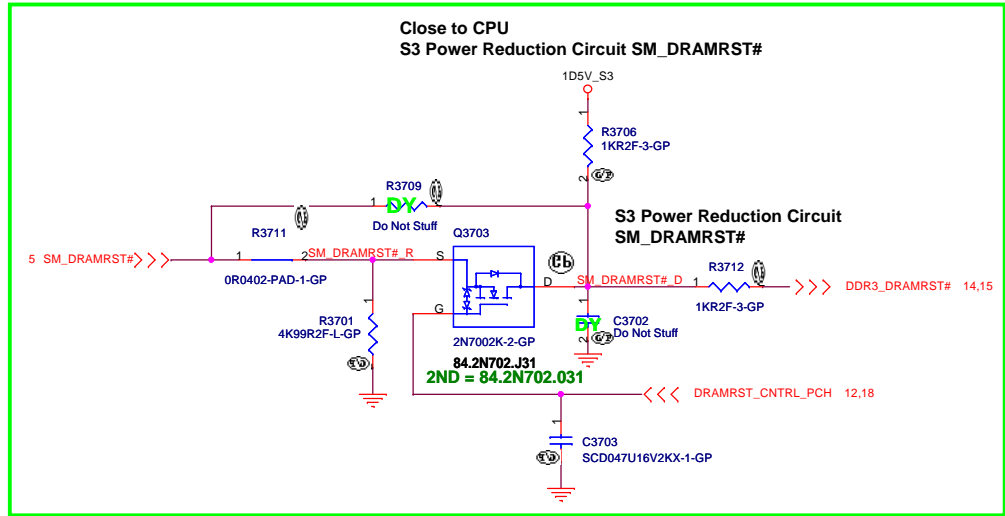
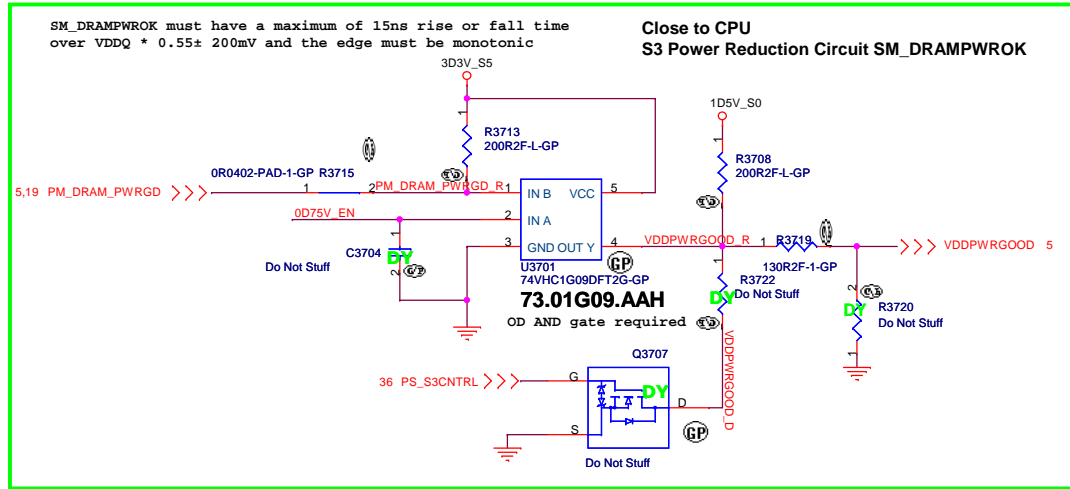


BOM1

緯創資通 Wistron Corporation

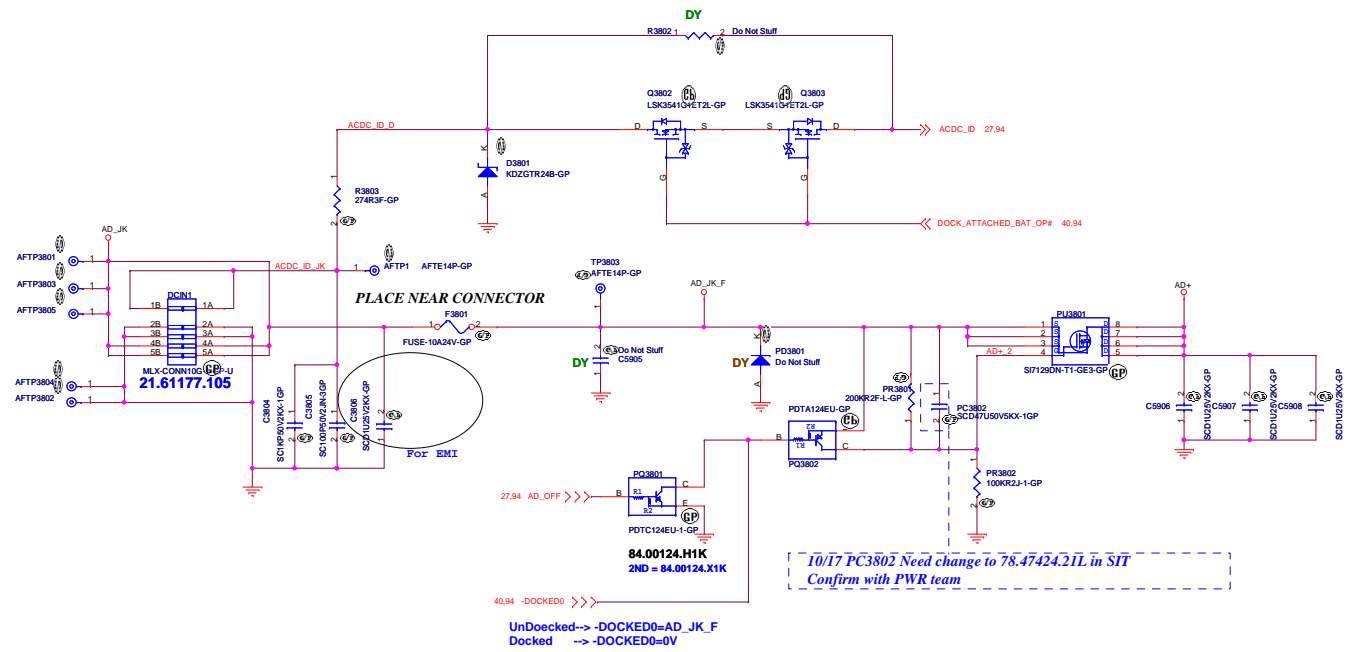
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
Power Plane Enable			
Size	Document Number	Rev	
A3	CD1 DIS	SC	
Date: Tuesday, December 13, 2011		Sheet 36	of 102

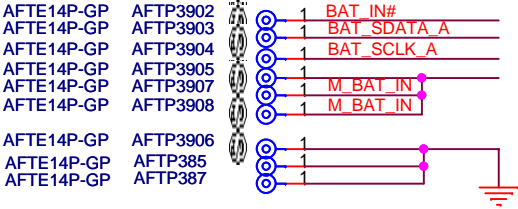
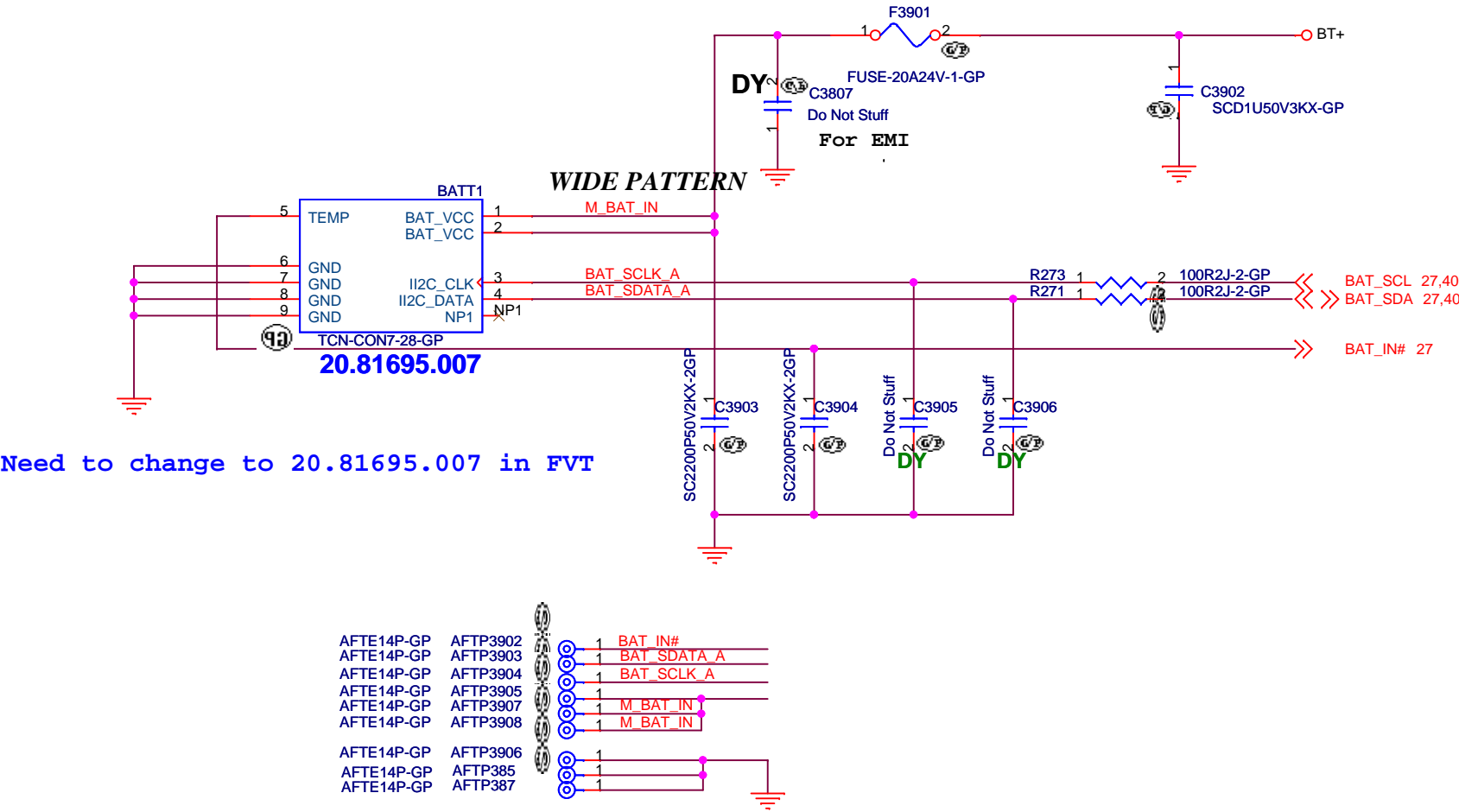


BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size A3	
Document Number	
Date: Tuesday, December 13, 2011	
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Rev SC	
ADAPTER	
CD1 DIS	



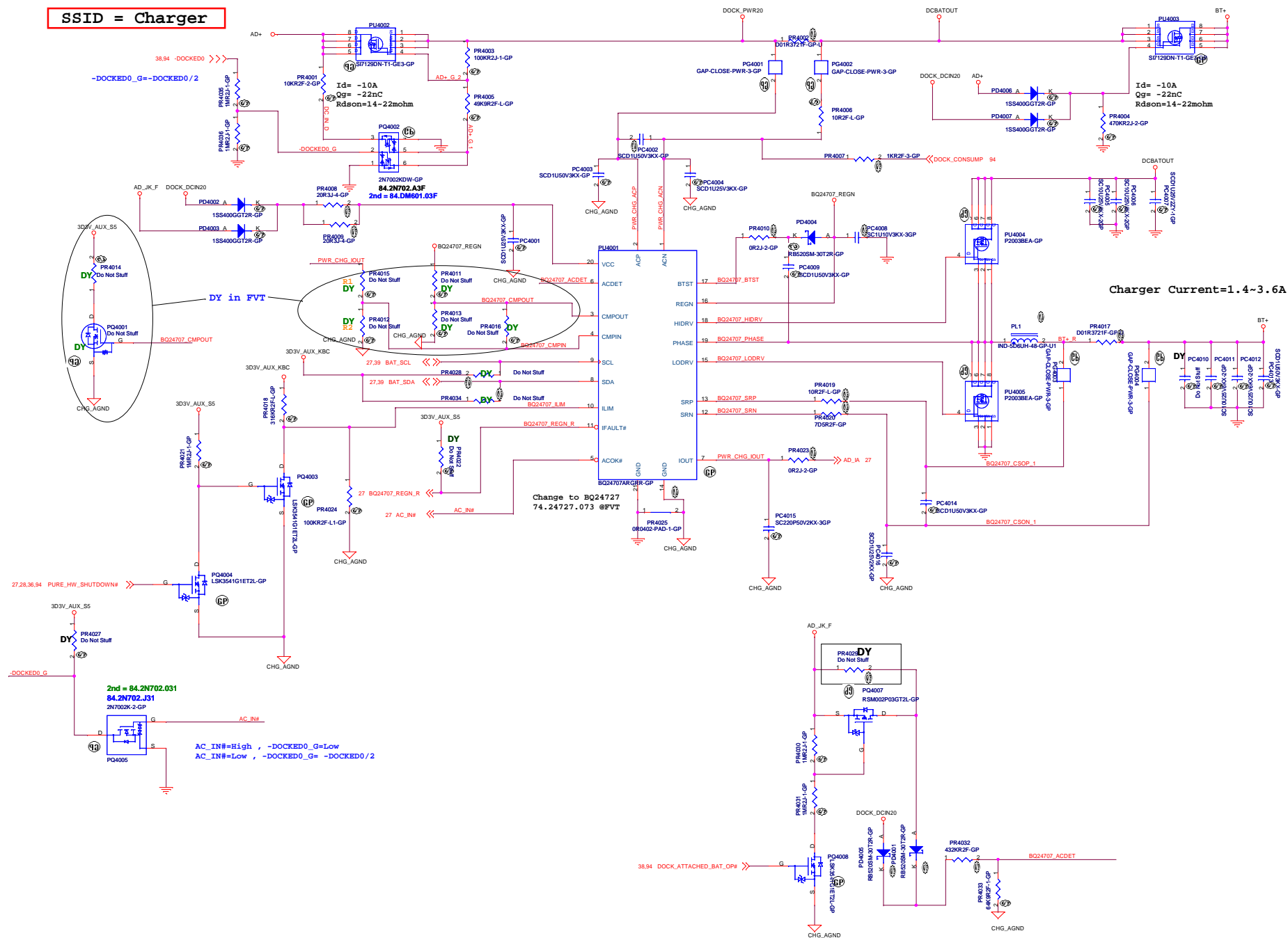
BATT Connector



BOM1

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BATT CONN			
Size A4	Document Number CD1 DIS		Rev SC
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SSID = Charger

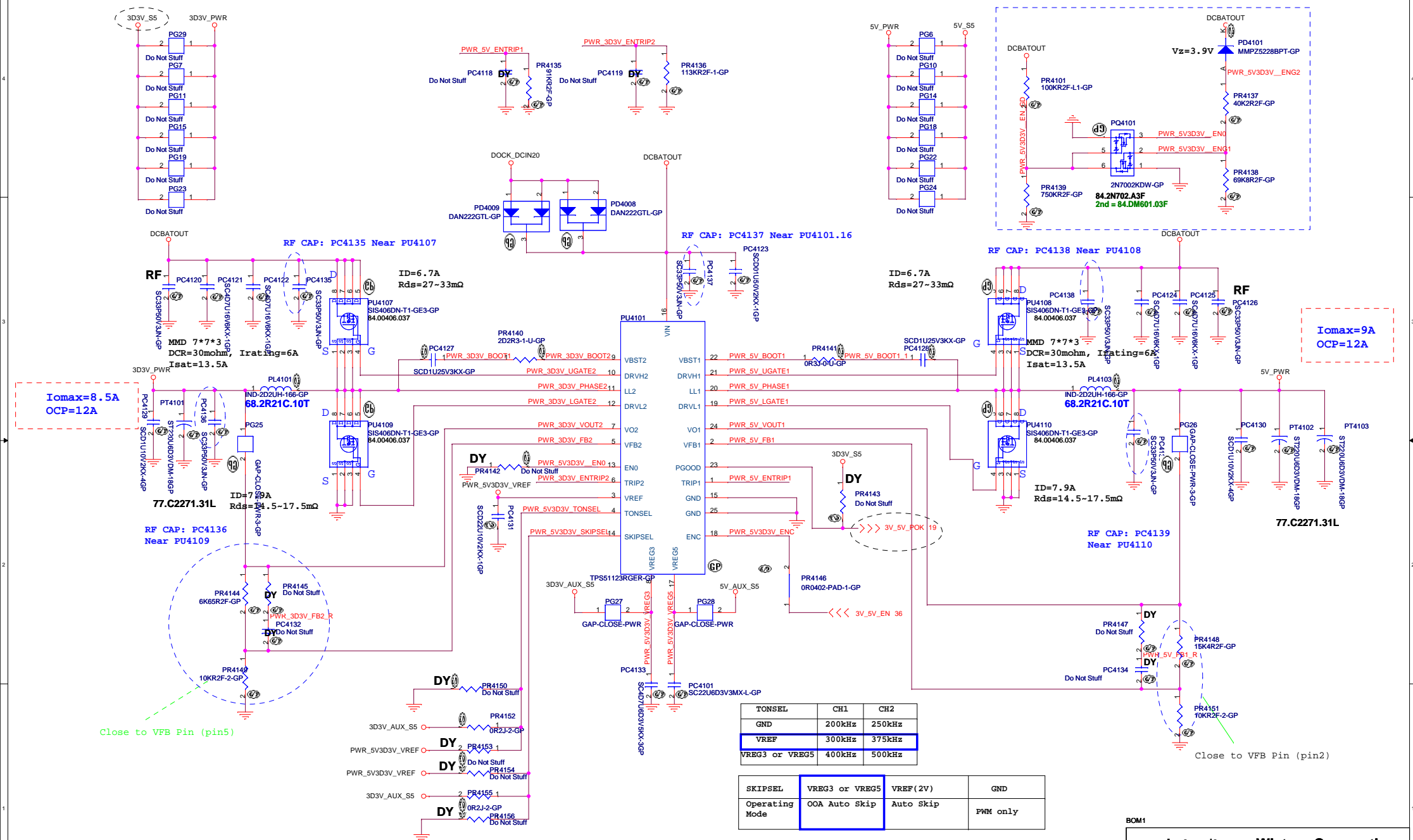


BOM1

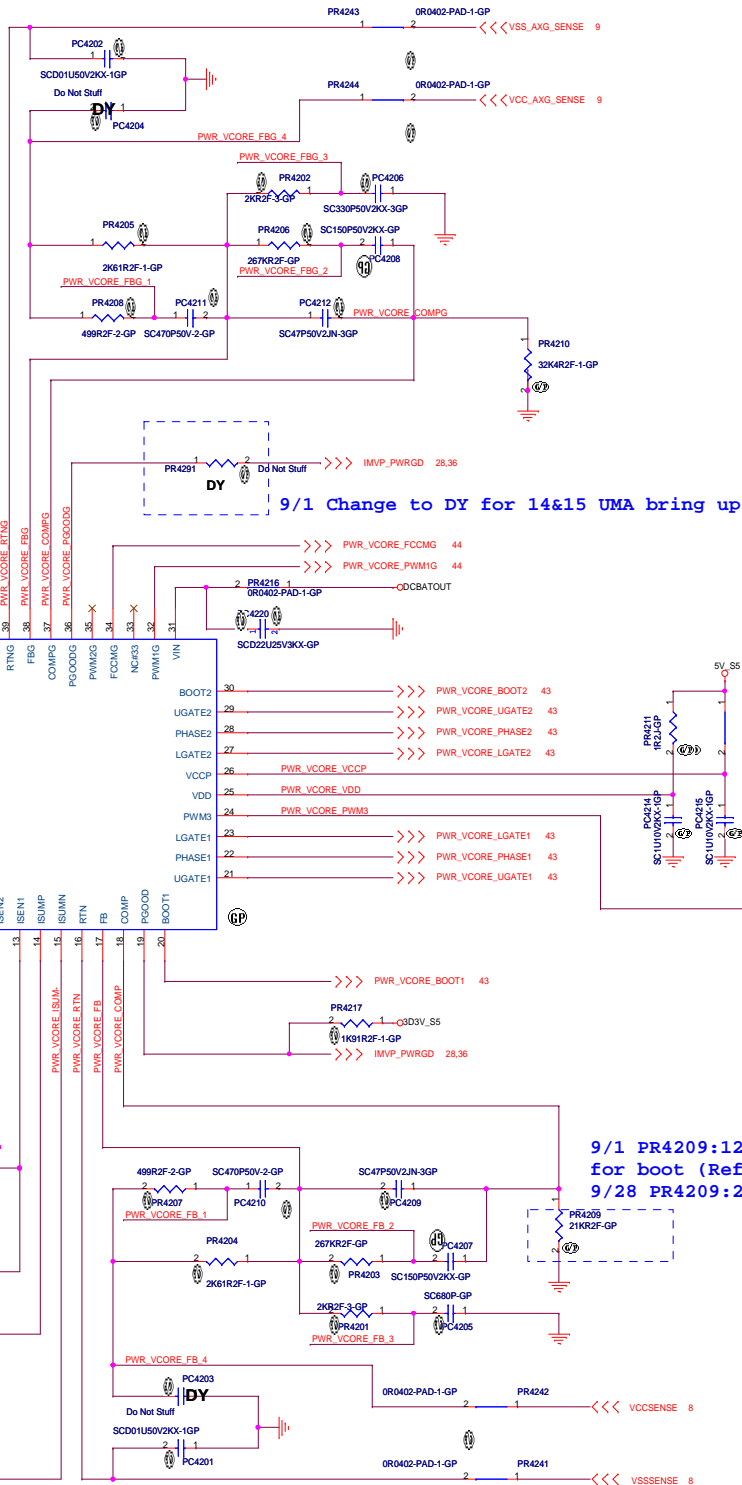
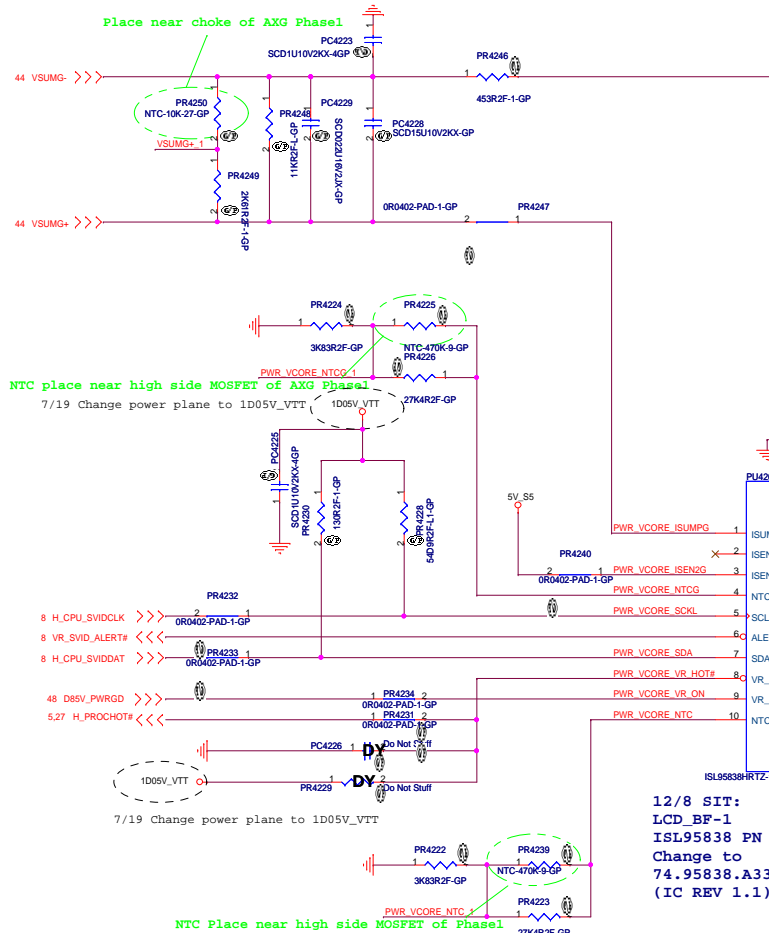
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

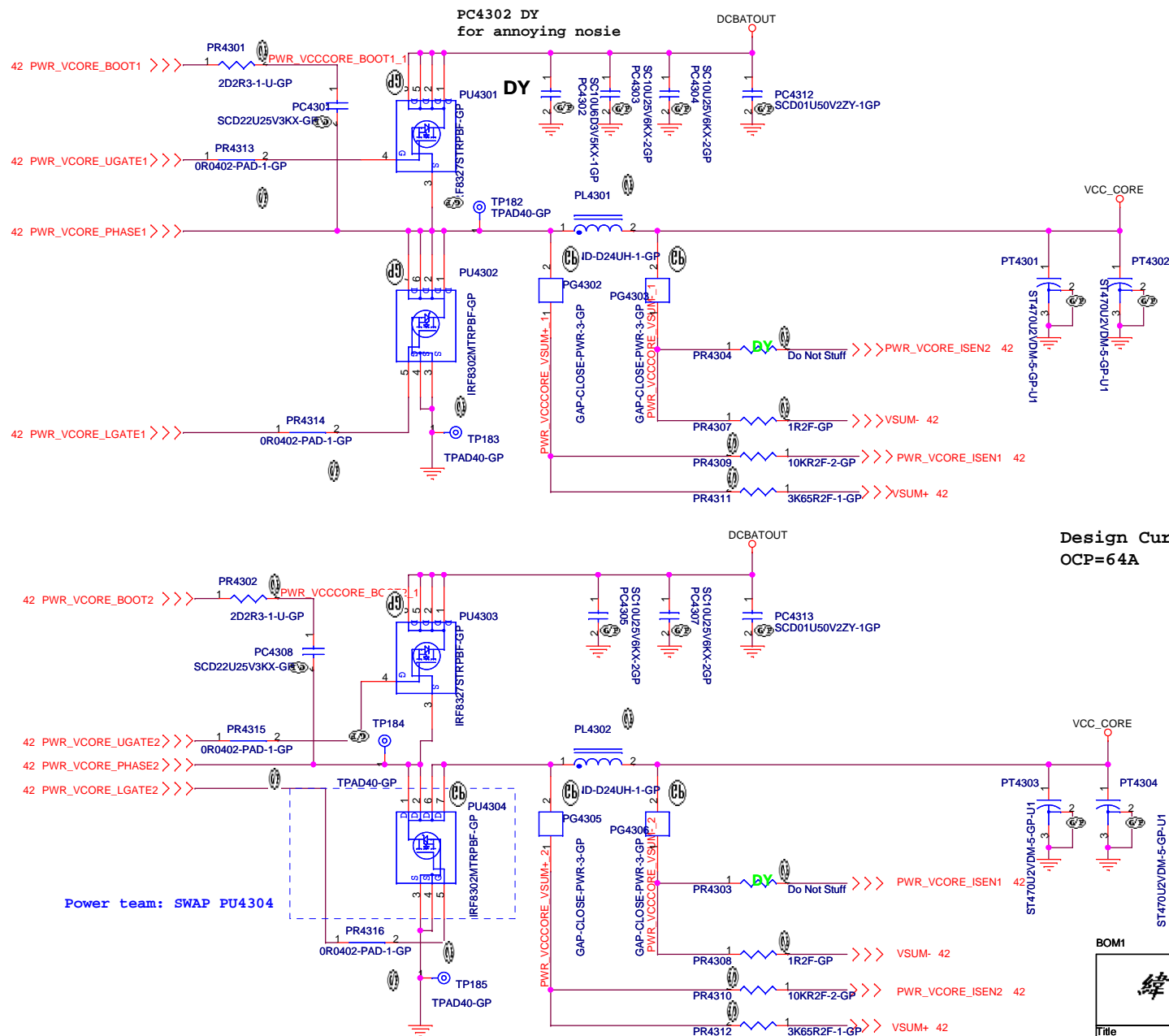
Title				CHARGER			
Size	Document Number					Rev	
	CD1 DIS						SC
Date: Tuesday, December 13, 2011				Sheet 40 of 102			

Confirm PWR for PQ4101 circuit Fun. (FVT Stage)



BOM1





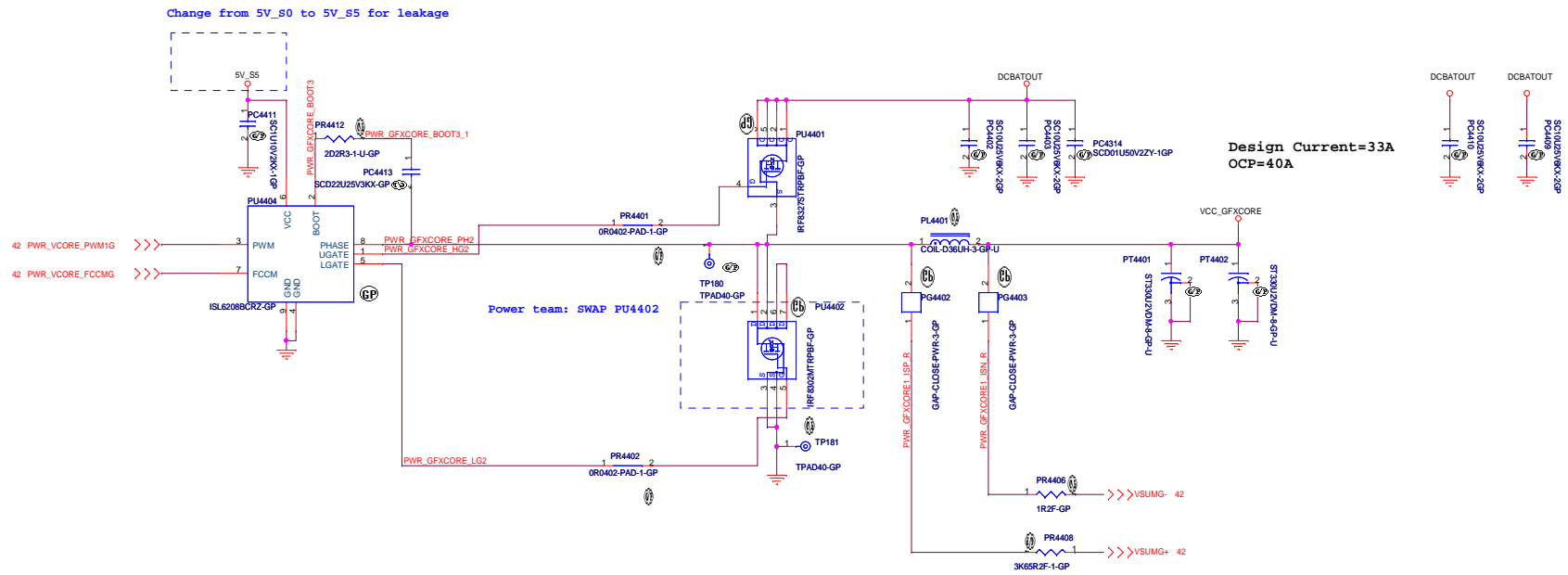
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BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU CORE		
Size B	Document Number	Rev
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Date: Tuesday, December 13, 2011	Sheet 43	of 102

```
SSID = AXG.Regulator
```



Design Current=33A
OCP=40A

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU CORE

Size

Document Number

CD1 DIS

Rev	
-----	--

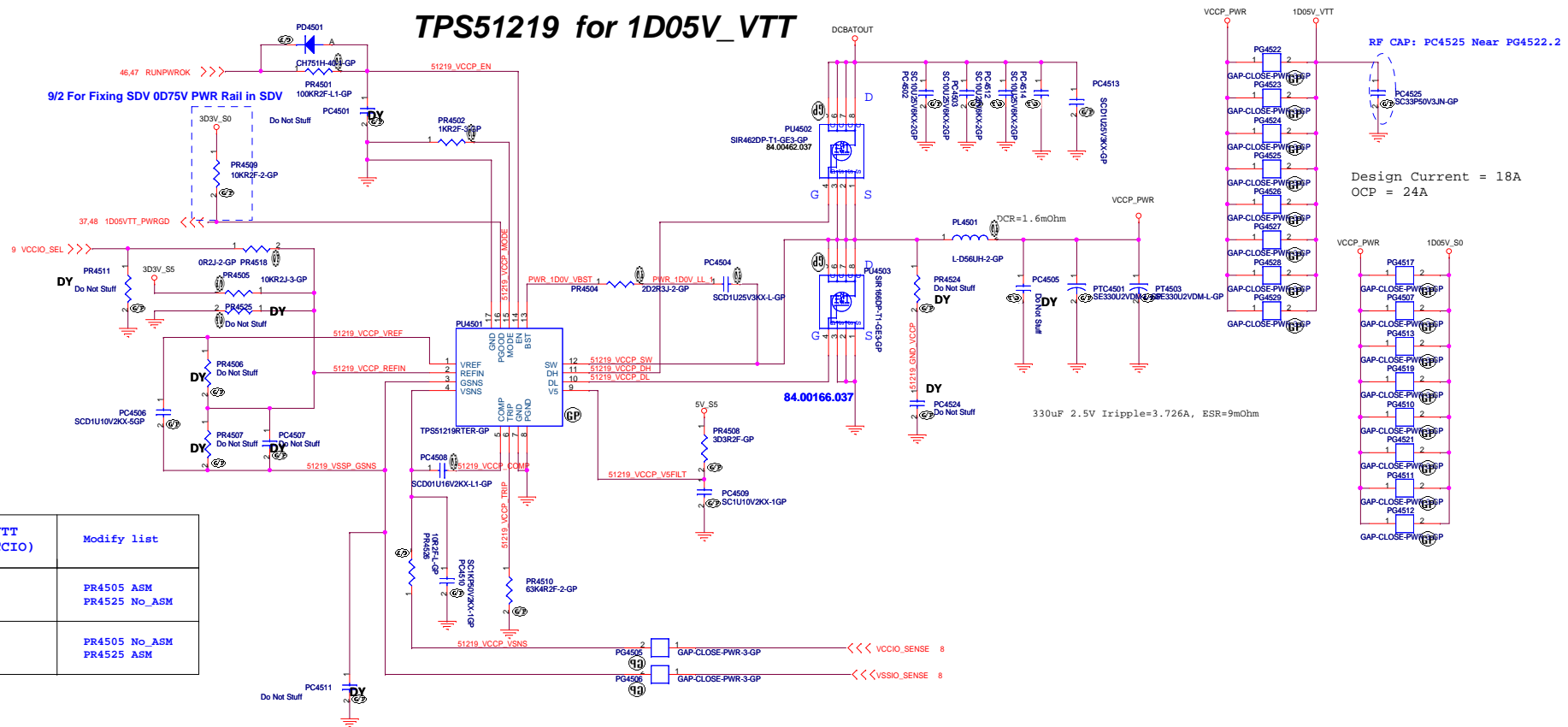
SC

Date: Tuesday, December 13, 2011

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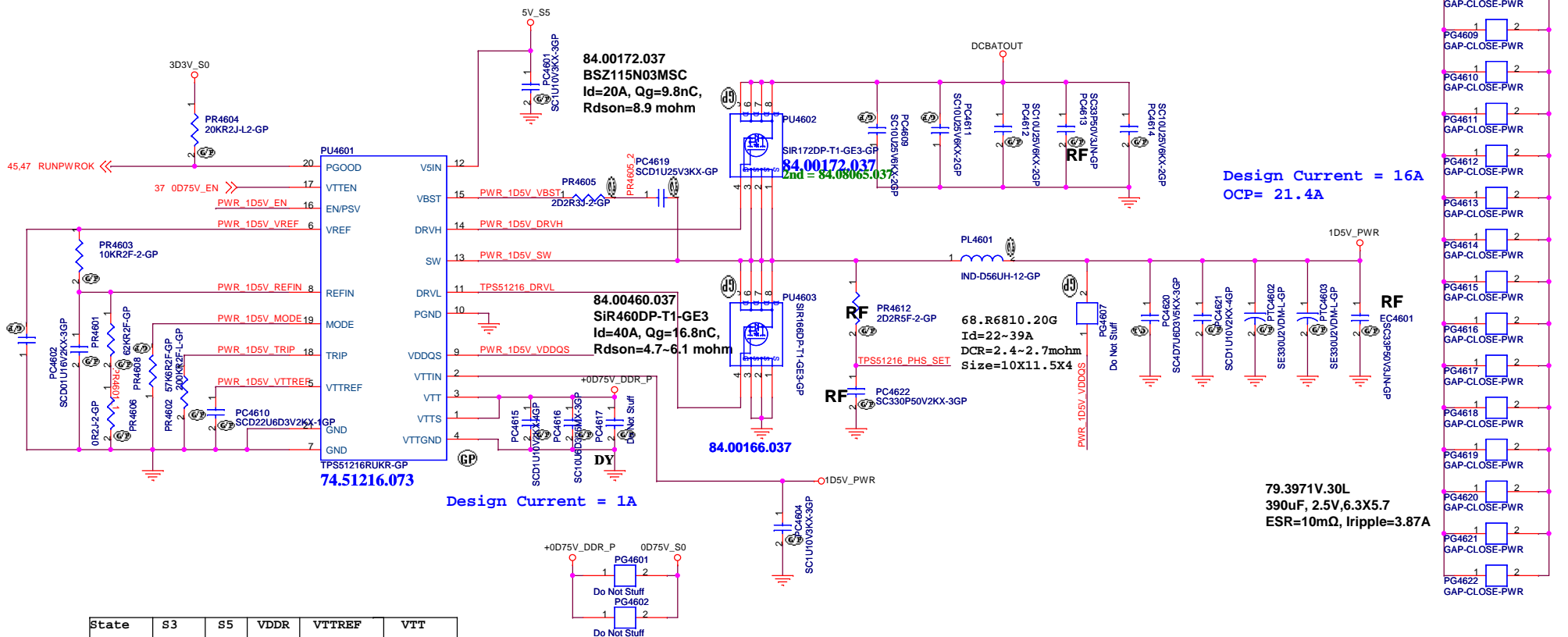
102

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TPS51219 for 1D05V_VTT

1D05V_VTT (CPU VCCIO)	Modify list
1.05V	PR4505_ASM PR4525_No_ASM
1.0V	PR4505_No_ASM PR4525_ASM

SSID = PWR.Plane.Regulator 1p5v0p75v

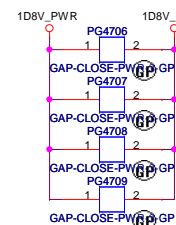
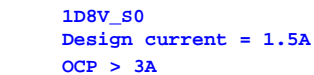


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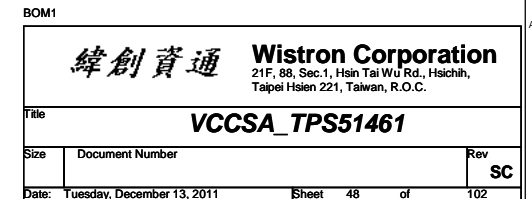
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51216 1D5V&0D75V
Size A3 Document Number
CD1 DIS
Date: Tuesday, December 13, 2011 Sheet 46 of 102

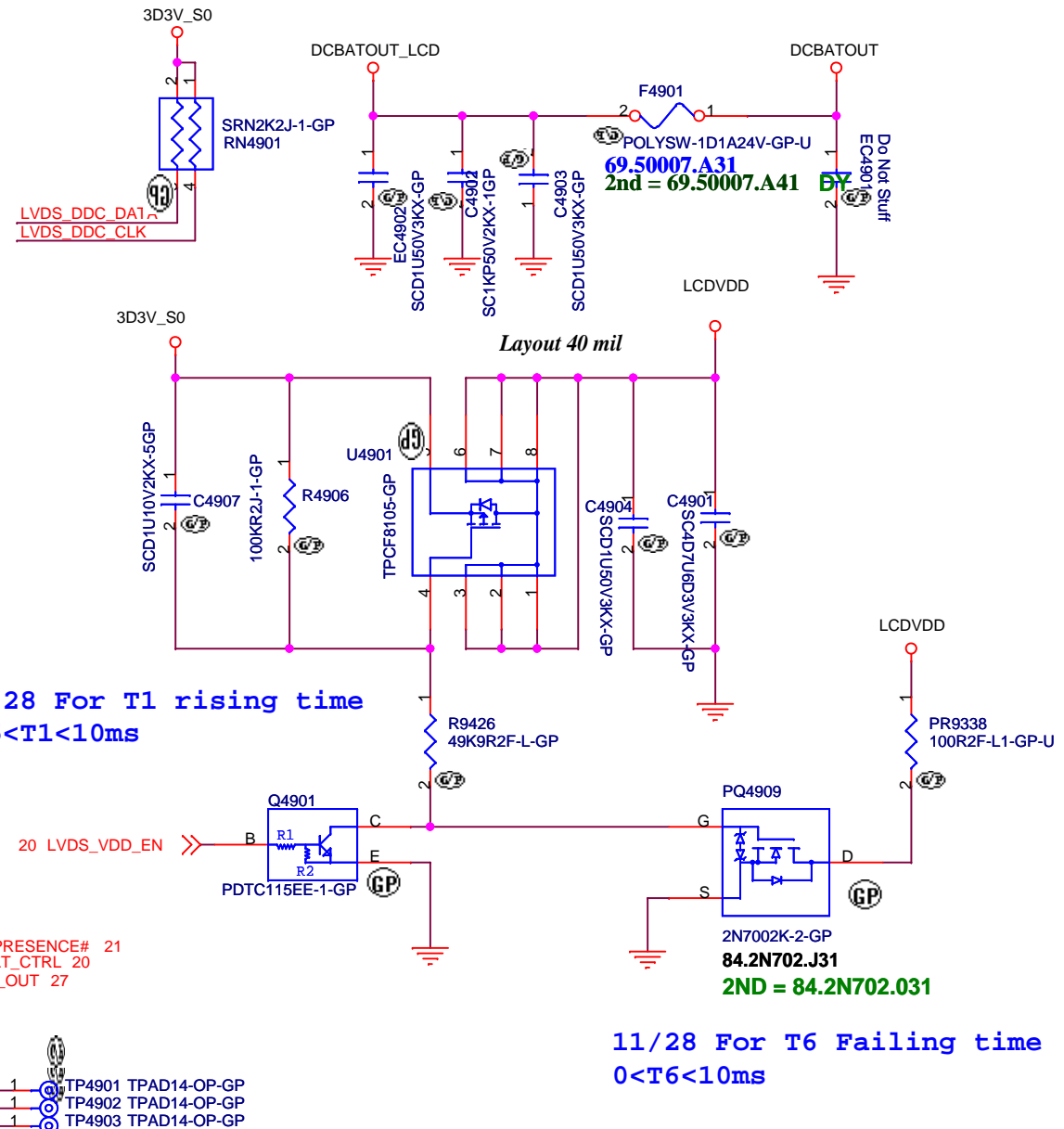
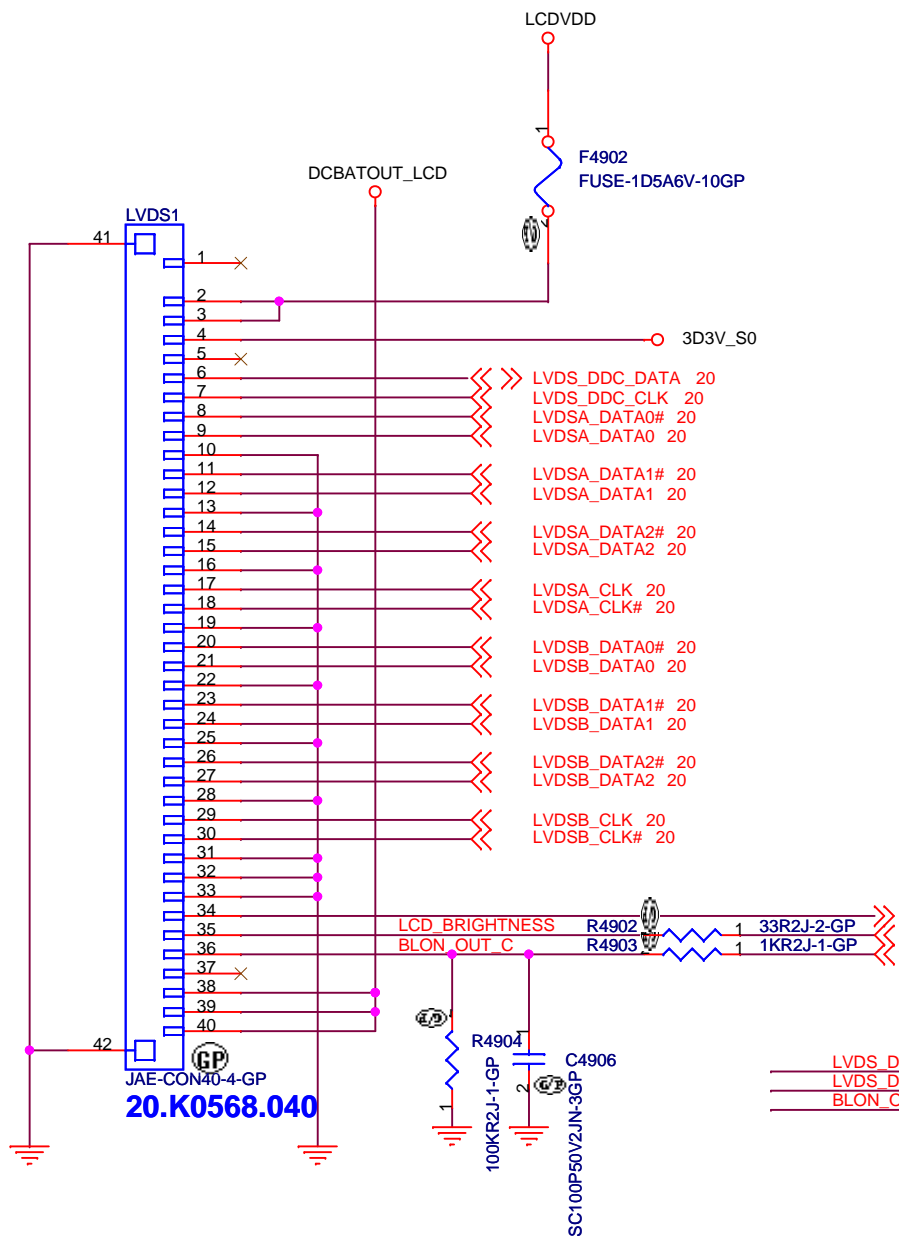
TPS51311 for 1D8V_S0



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LVDS CONNECTOR



BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
LCD Connector	
Size A4	Document Number CD1 DIS
Date: Tuesday, December 13, 2011	Rev SC
Sheet 49	of 102

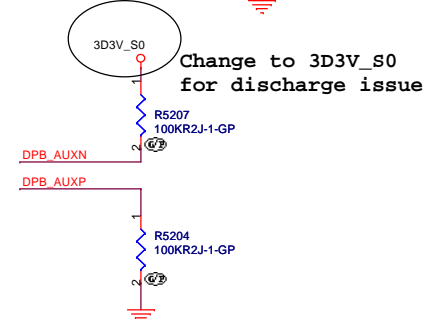
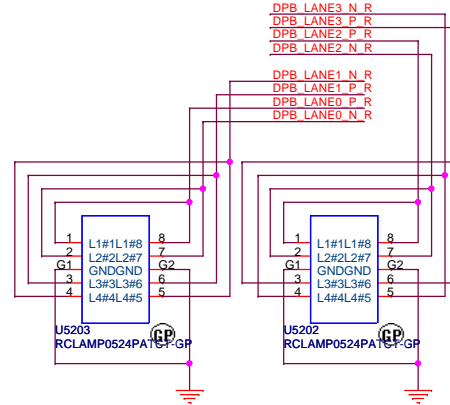
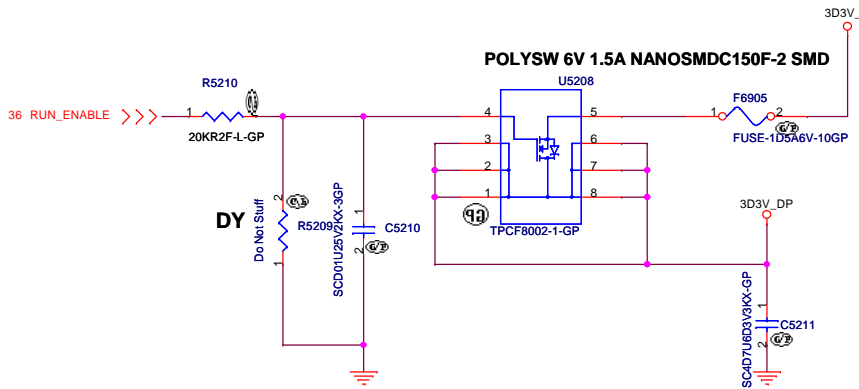
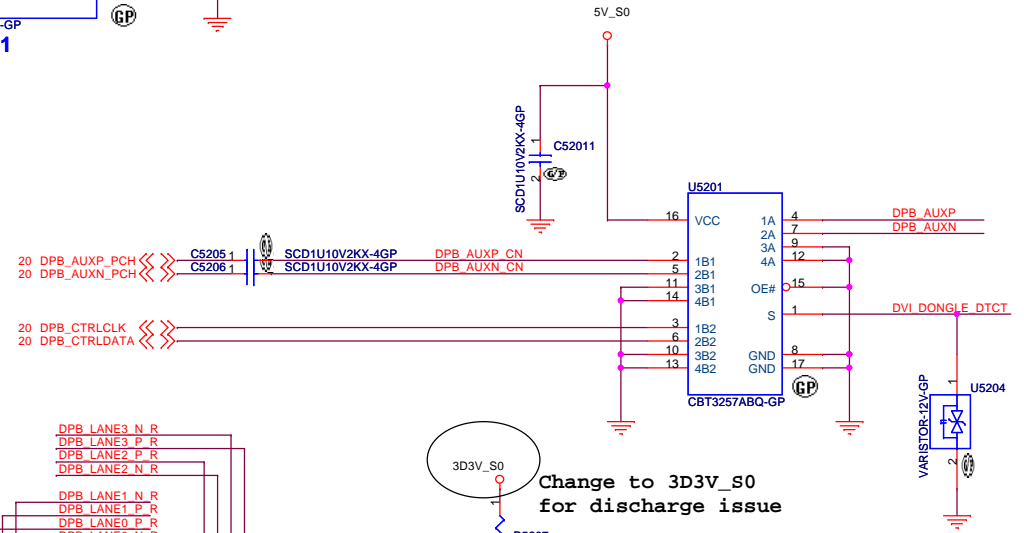
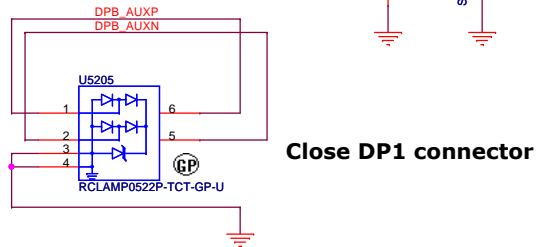
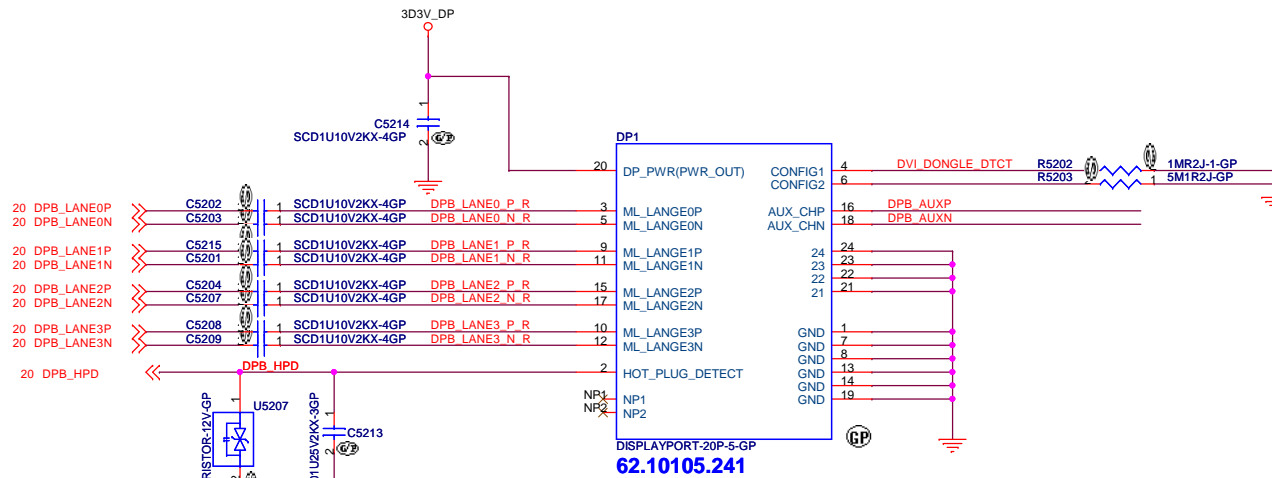
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BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
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<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A3</div>	<div>CD1 DIS</div>		<div>SC</div>
<div>Date:</div>	<div>Tuesday, December 13, 2011</div>	<div>Sheet</div>	<div>51 of 102</div>

1

Mini Display Port Connector



BOM1

緯創資通 Wistron Corporation

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Title

Display Port

Size A3 Document Number CD1 DIS

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Rev SC

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BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
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BOM1

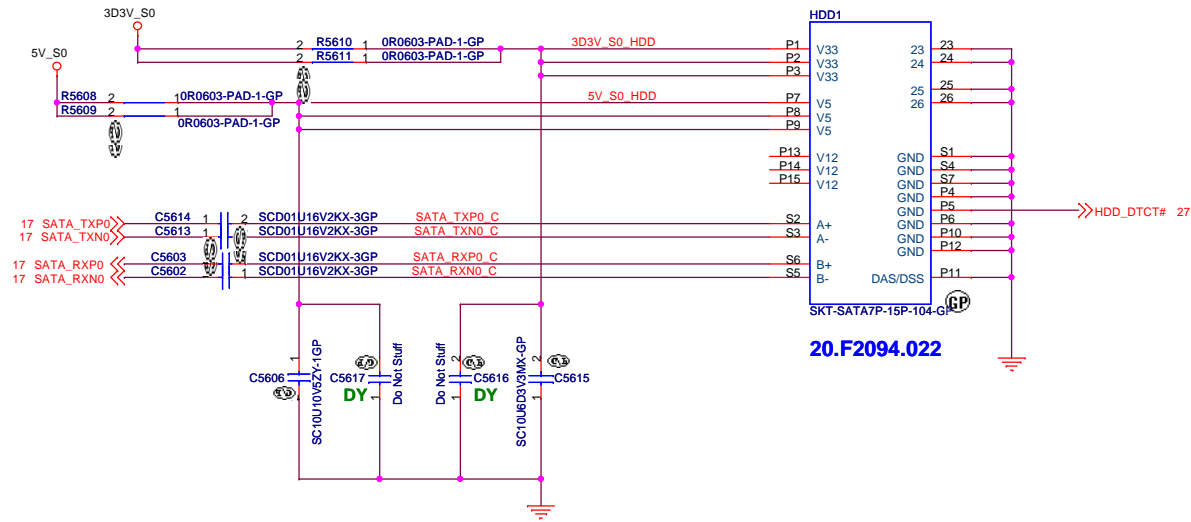
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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BOM1

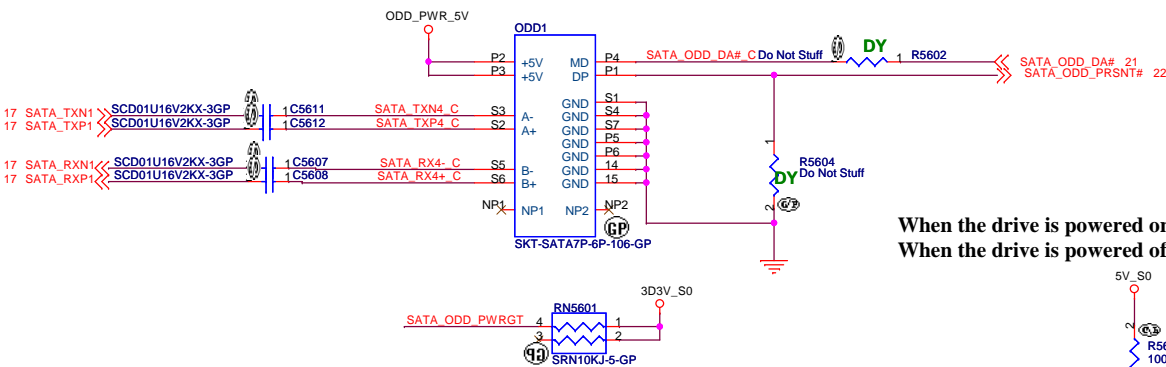
<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>	<div>Rev</div>	<div>SC</div>
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		<div>1</div>	

SATA HDD Connector



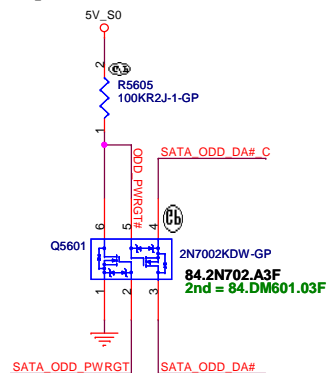
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



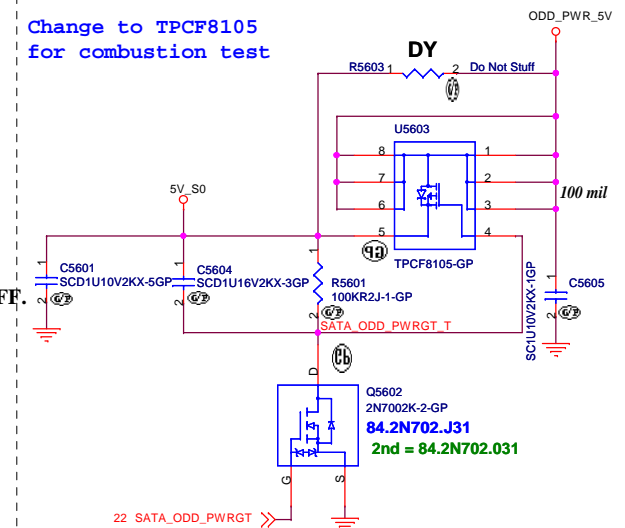
SUPPORT ZERO SATA ODD

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD

Change to TPCF8105
for combustion test



BOM1

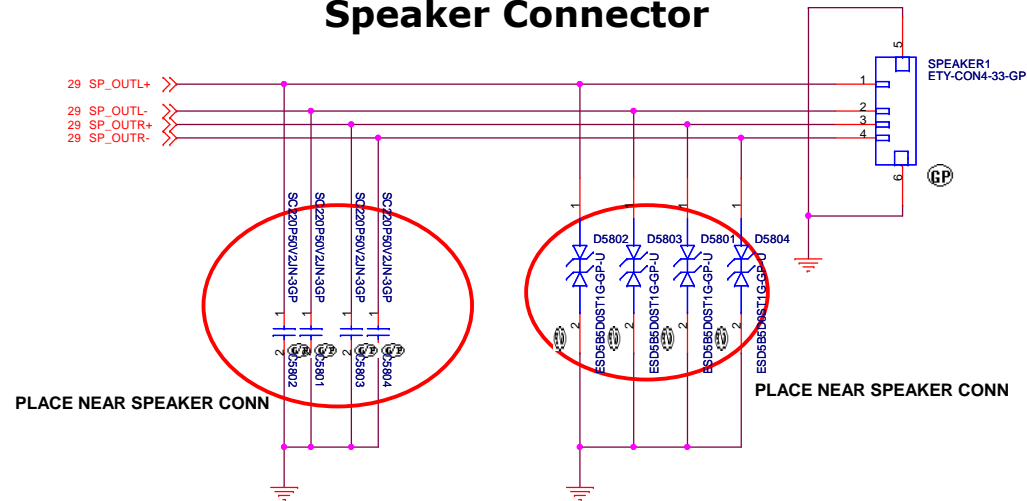
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD/ODD			
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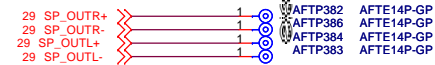
BOM1

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		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>RESERVED</div>			
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Speaker Connector



Near SPEAKER1 Speaker



BOM1

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Title

SPEAKER CONN

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A3

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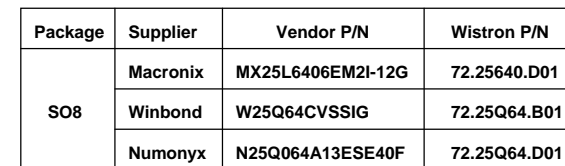
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8M SPI ROM for Commercer



Title			
Flash/RTC			
Size A3	Document Number CD1 DIS		Rev SC
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SSID = USB

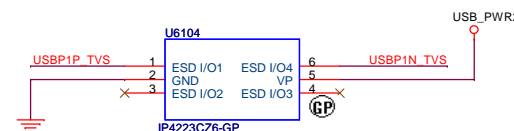
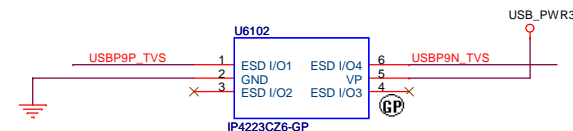
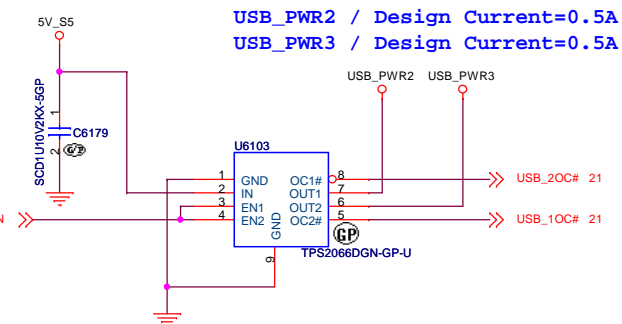
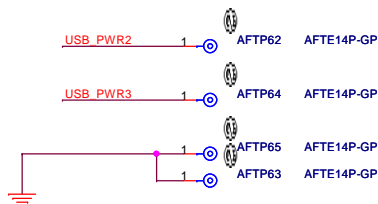
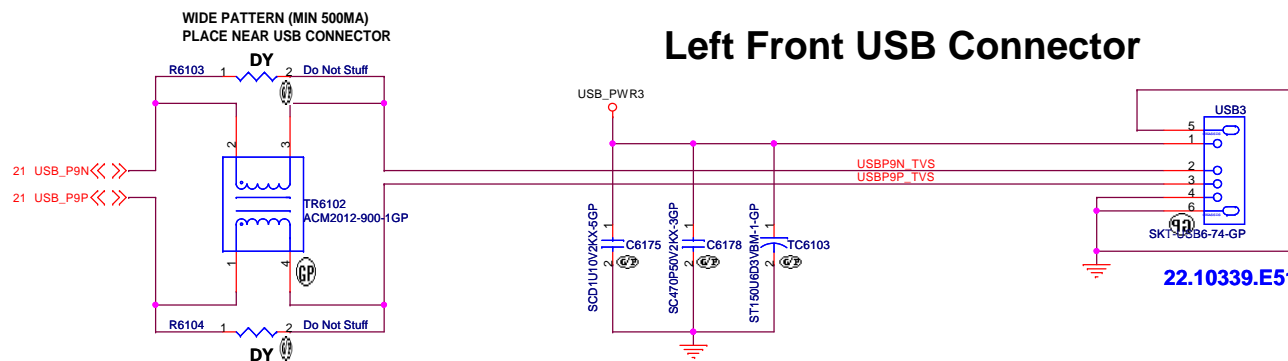
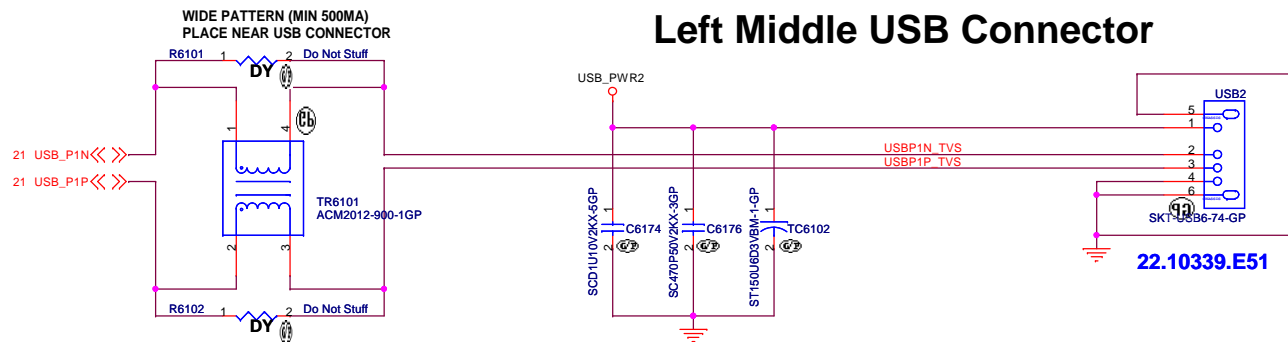


Table 61.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2066DGN	41R0511AA	74.02066.A71
TI	TPS2066DGN-1	N/A	74.02066.B71

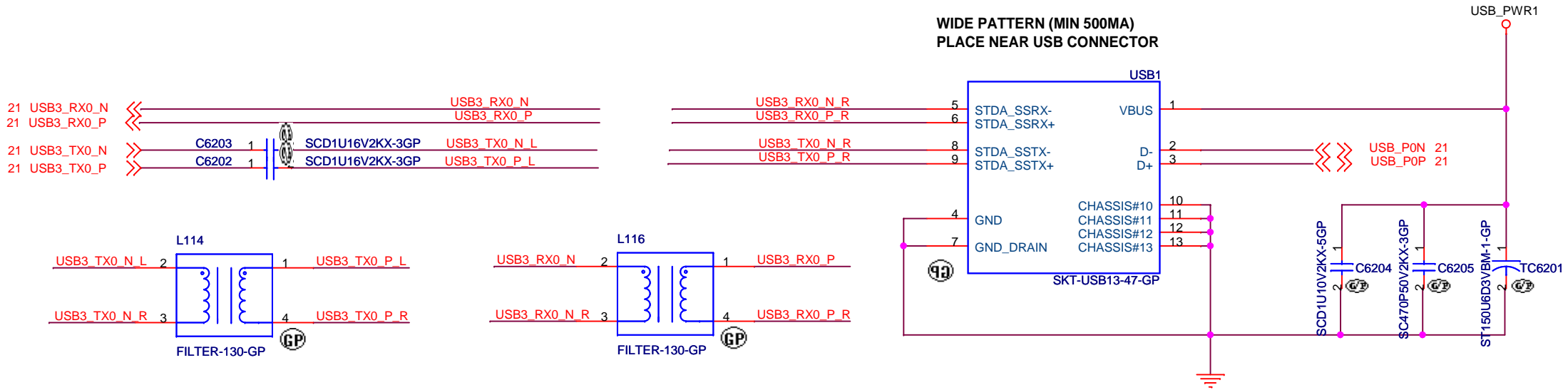
Table 61.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

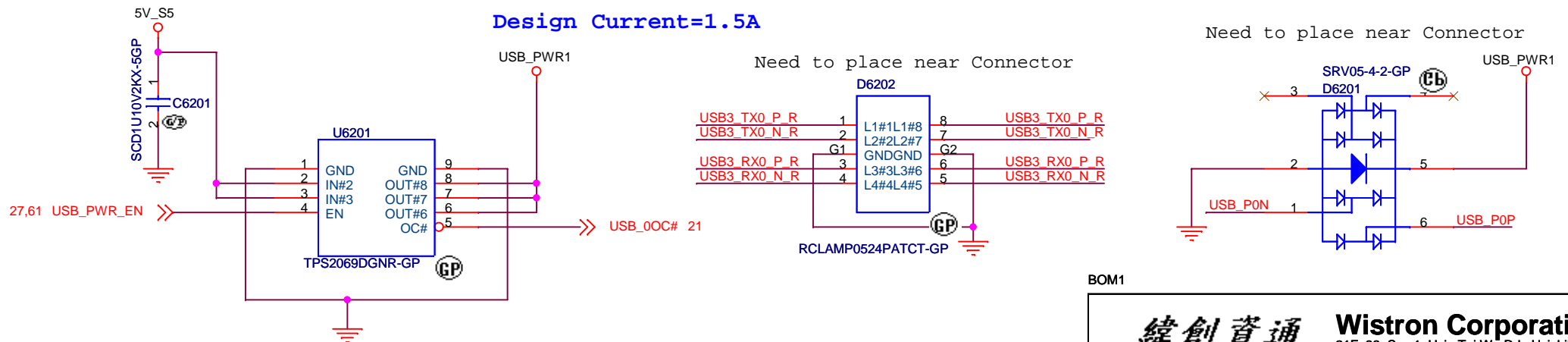
Table 61.3- ESD protection

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	IP4223CZ6	N/A	83.42236.0AE
AOS	AOZ8904CIL	N/A	83.08904.0AE
AMC	AZC099-04S	N/A	83.09904.AAE

Left Rear USB Connector



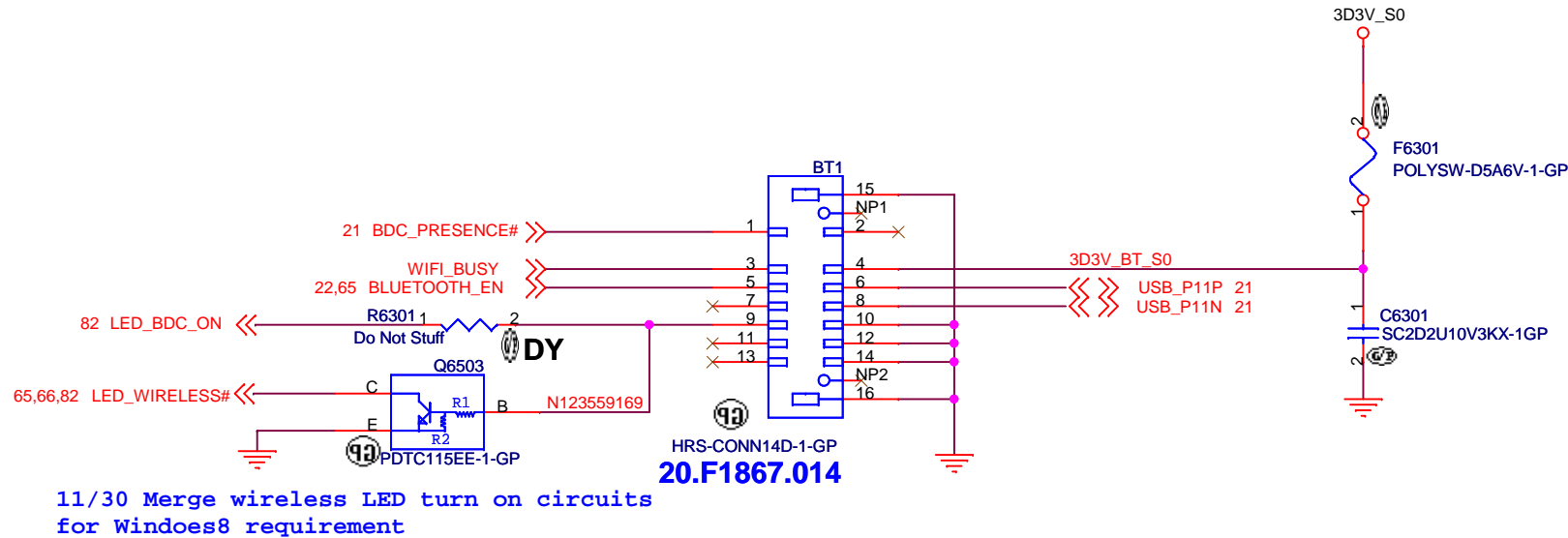
L114/L116 add for EMI



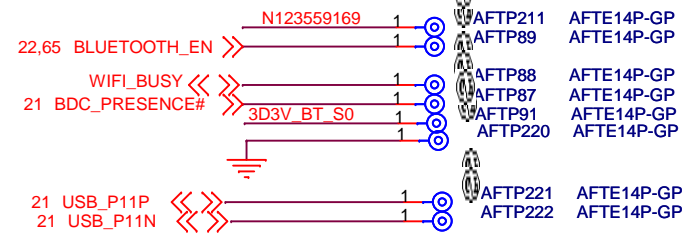
BOM1

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USB3.0	
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Bluetooth Module conn.



Near BT1 BDC CONNECTOR



BOM1

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Bluetooth			
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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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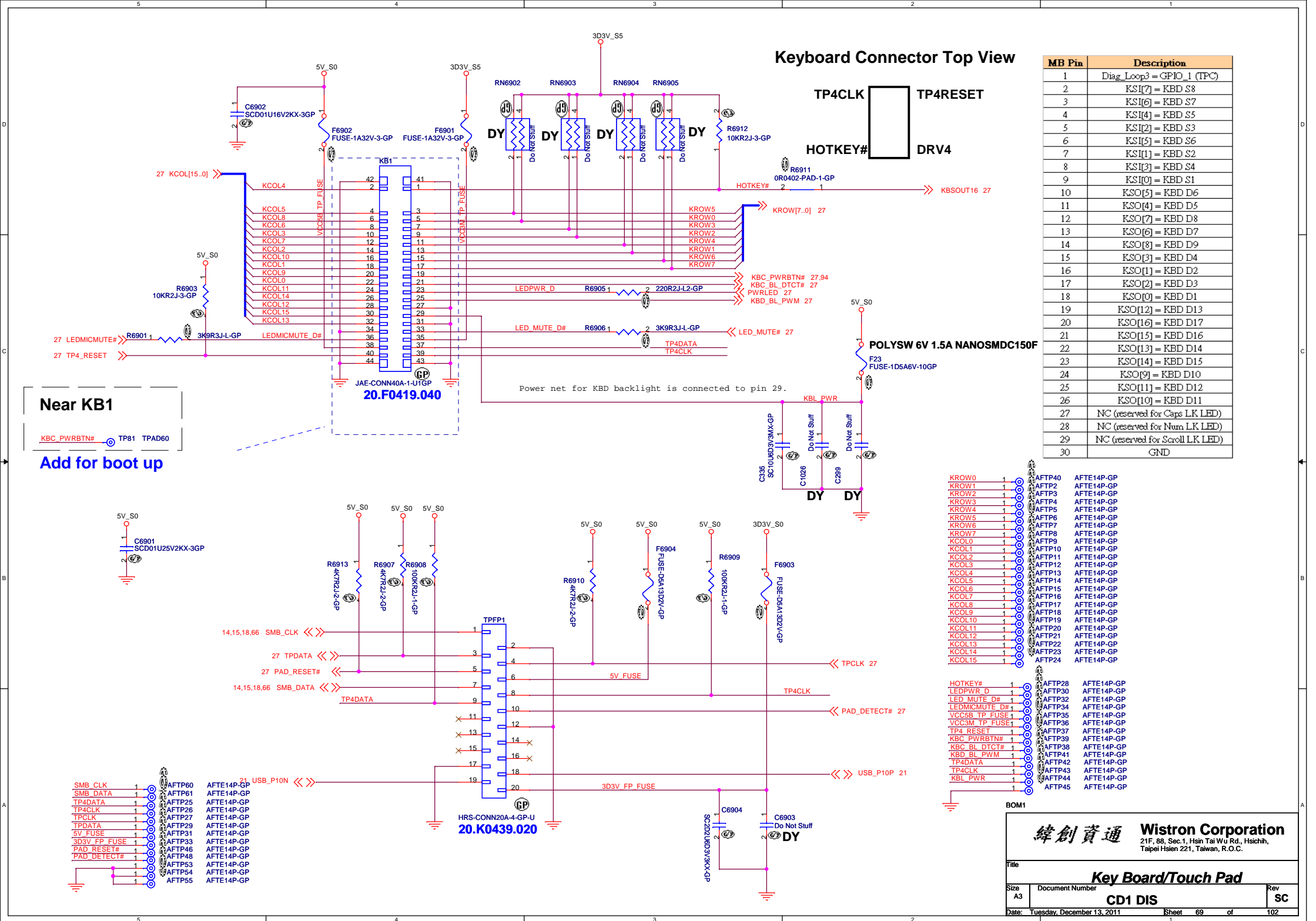
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BOM1

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Title		
LED Bard/Power Button		
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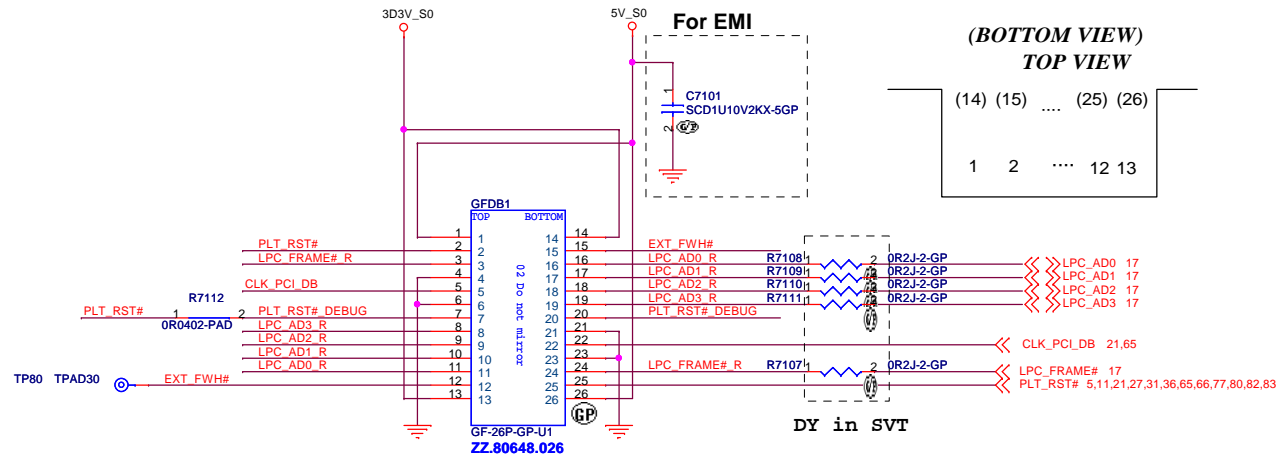


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<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Hall Sensor</div>		
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Golden Finger for Debug Board



BOM1

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<div>Reserved</div>			
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1

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20.I0129.001			
Pin	TYPE	FUNCTION	RTS5138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

BOM1

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SD/XD/MS/MMC Card CONN

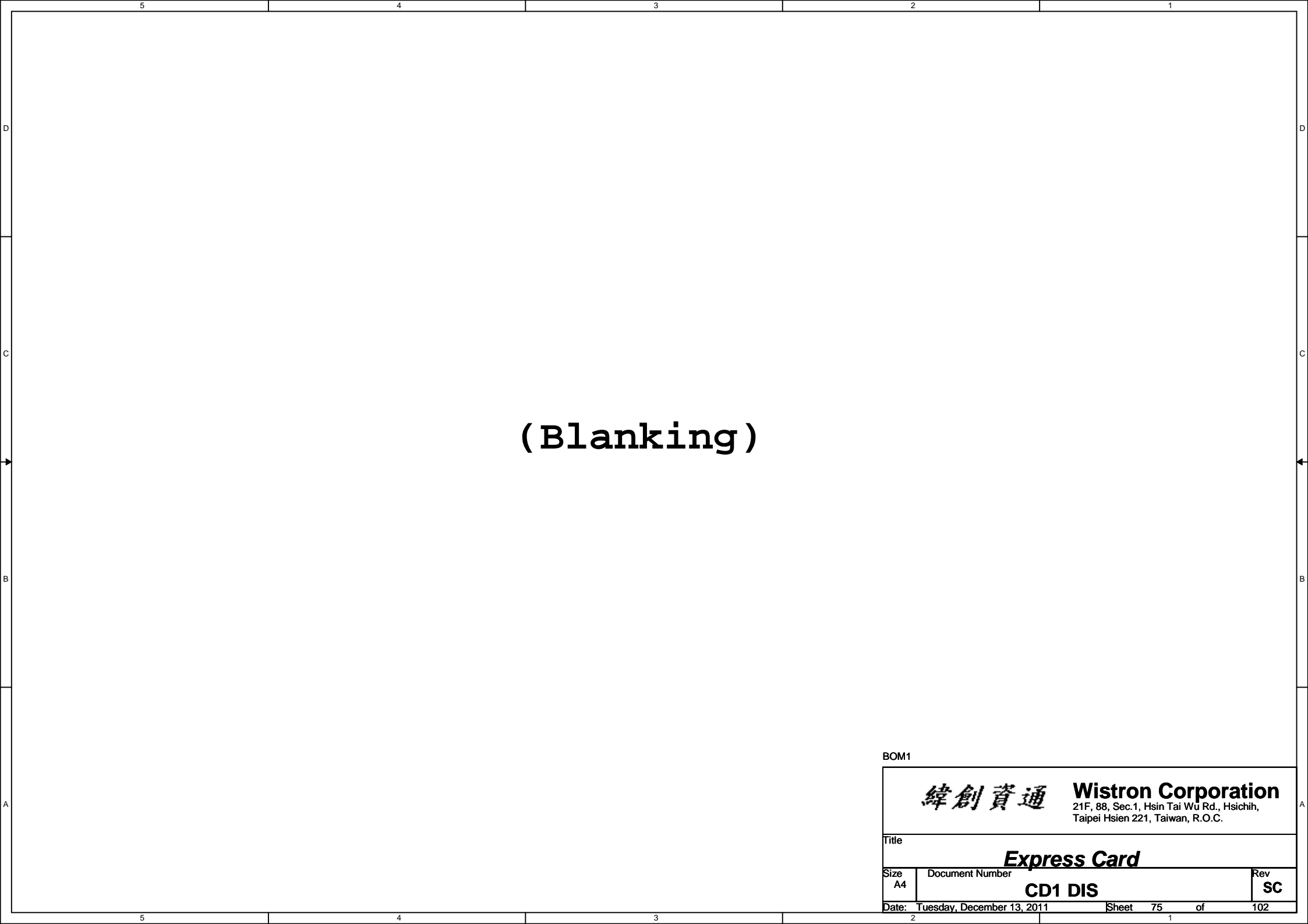
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Title	
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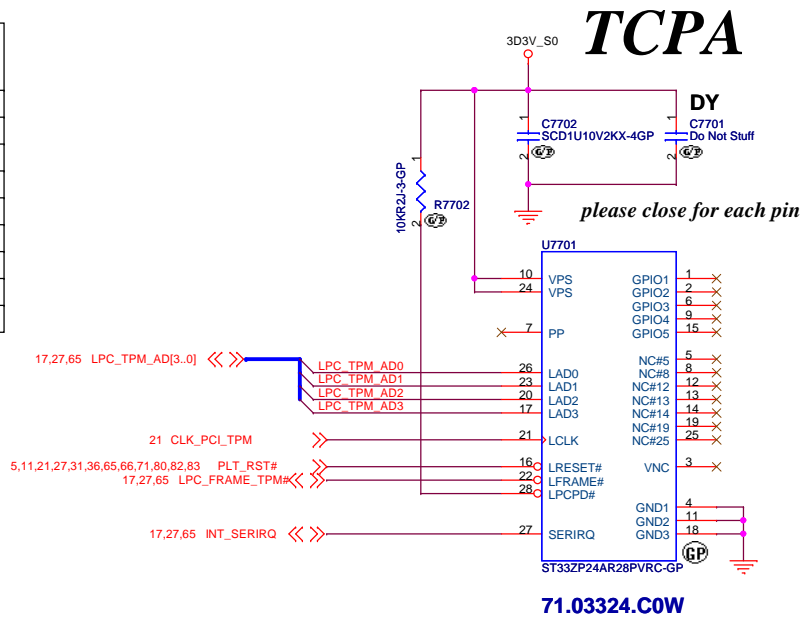
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	NO TPM	ST Micro ST19NP18ER28PVMK
U39	NO_ASM	ASM
C379	NO_ASM	ASM
C9203	NO_ASM	NO_ASM
R149	NO_ASM	ASM
R212	ASM	NO_ASM
R270	NO_ASM	ASM

↑
LOGIC



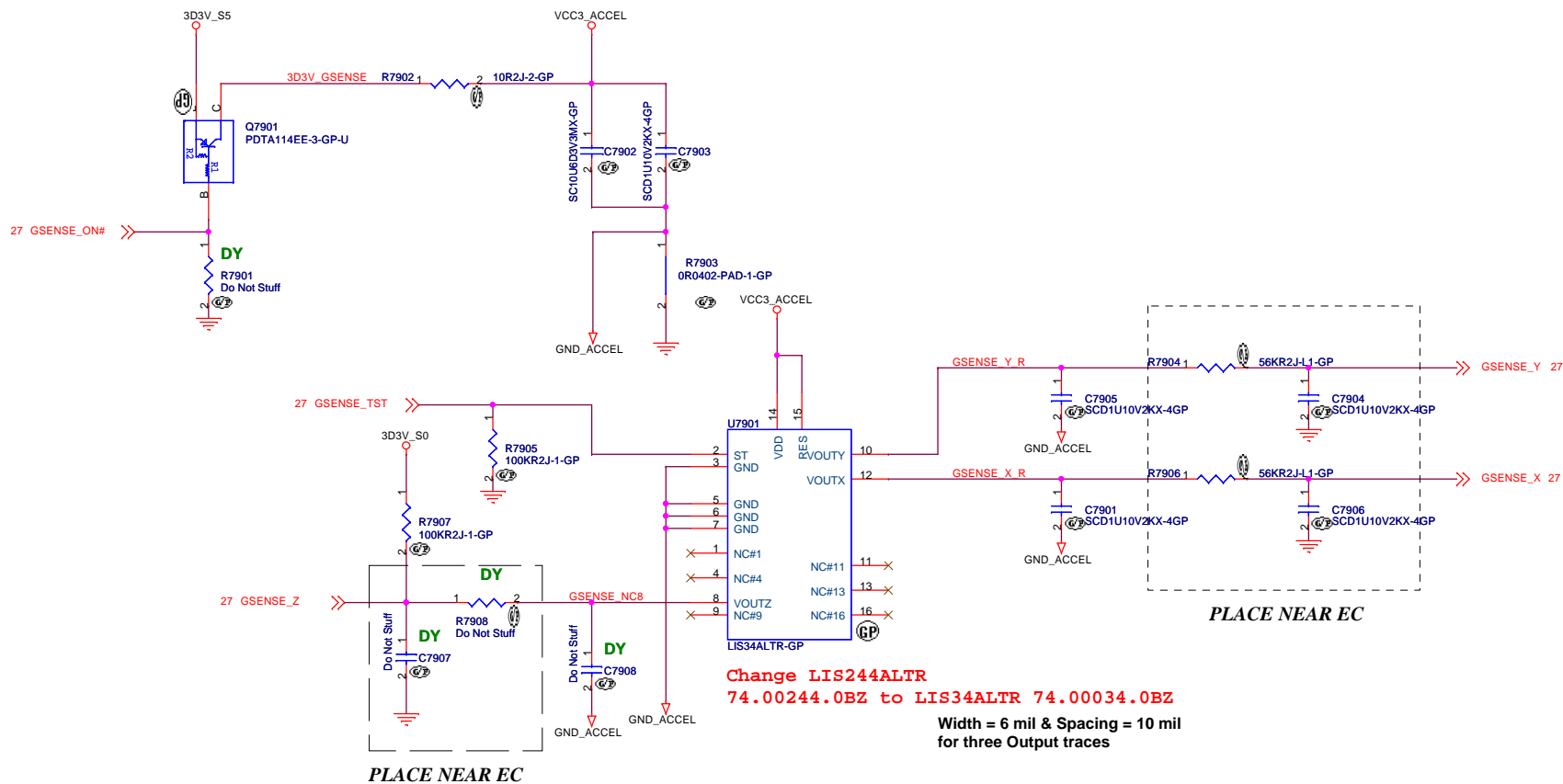
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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LIS244AL		NO ACC.
R401	NO-ASM	ASM
R957	ASM	ASM
U65	ASM	NO-ASM
Q105	ASM	NO-ASM
R885	10-OHM	NO-ASM
C829	ASM	NO-ASM
C969	ASM	NO-ASM
C830	ASM	NO-ASM
C847	ASM	NO-ASM
R970	56K	NO-ASM
C956	ASM	NO-ASM
R969	56K	NO-ASM
C938	ASM	NO-ASM
C704	NO-ASM	NO-ASM
R344	NO-ASM	NO-ASM
C703	NO-ASM	NO-ASM
R125	ASM	ASM

Table

	Supplier	Vendo P/N	WISTRON P/N
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2	Kionix	KXTC8-2850	74.KXTC8.0BZ

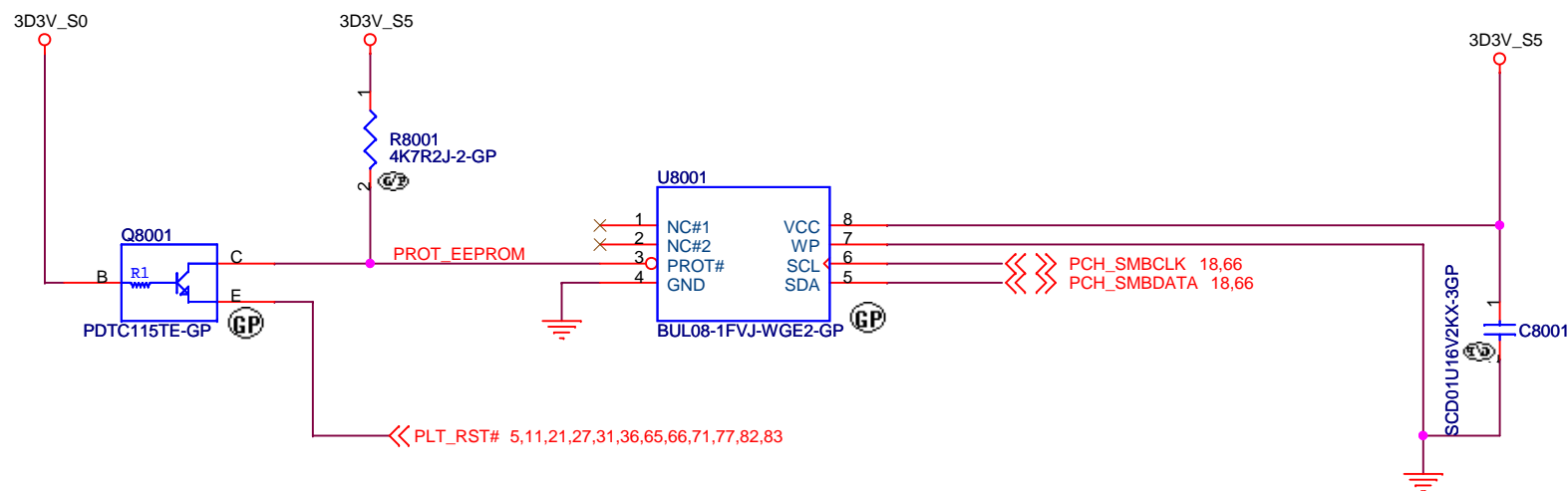
Layout Comment :

(1) Place C586, C588, Q17, R415, R417, C584, C585, R420 close to U34.

(2) Avoid routing under DCDC switching area.

BOM1

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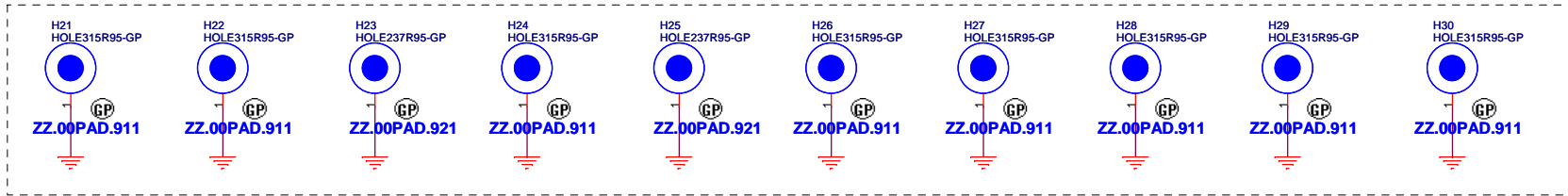
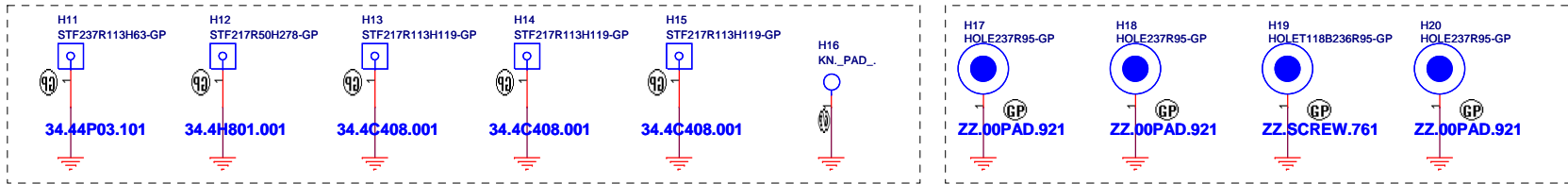
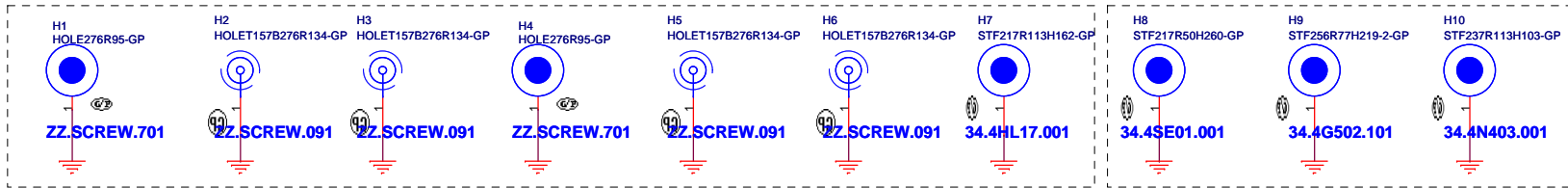


Supplier	Description	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	72.BUL08.A0Q
NXP	PCA24S08ADP	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	72.26C08.00R

BOM1

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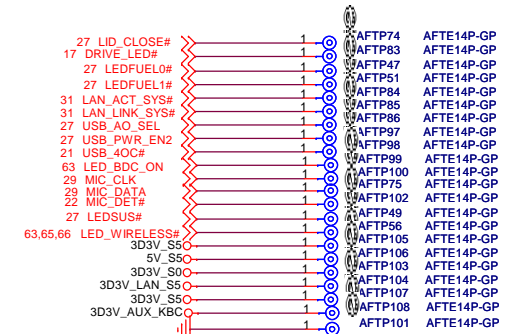
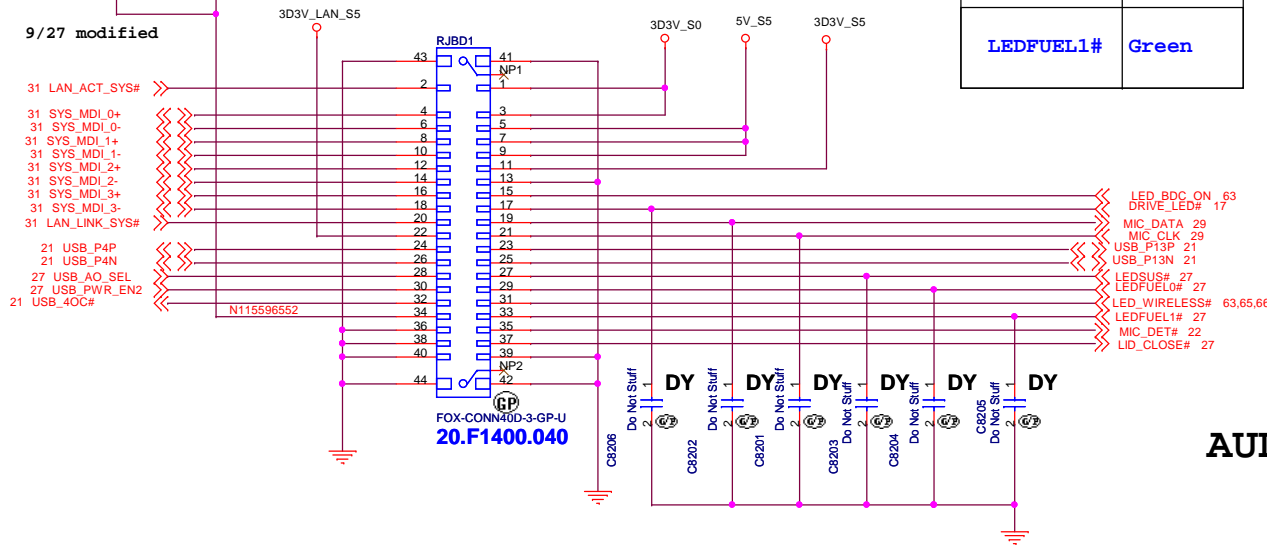
Reserve for
ISSC function
ECR105692

RJ45/AOU4/LED IF

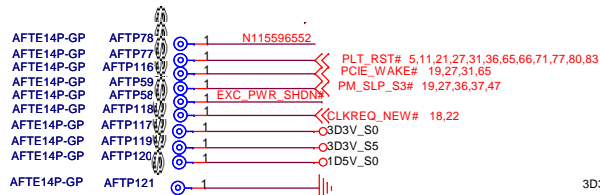
LED IF COLOR

LEDFUEL0#	Orange
LEDFUEL1#	Green

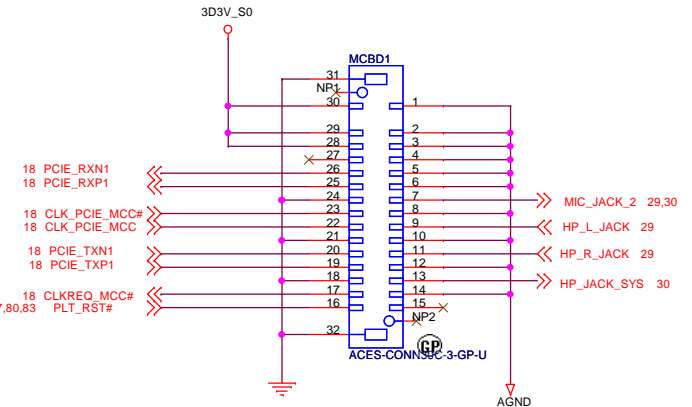
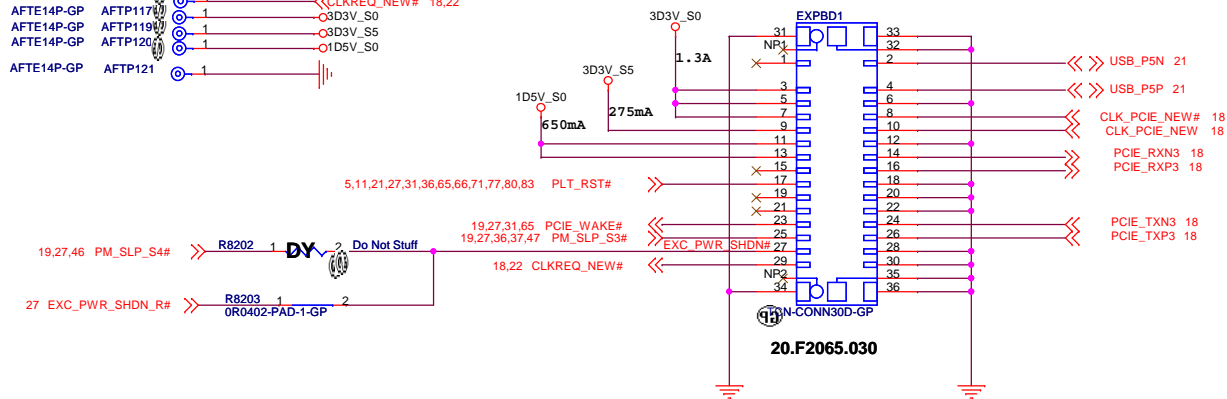
9/27 modified



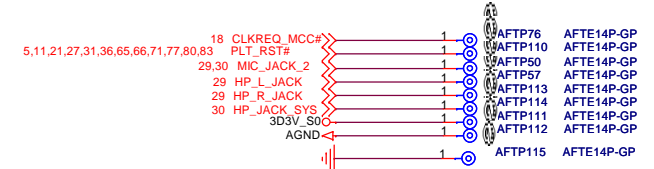
AUDIO JACK/MEDIA CARDREADER



EXPRESS CARD



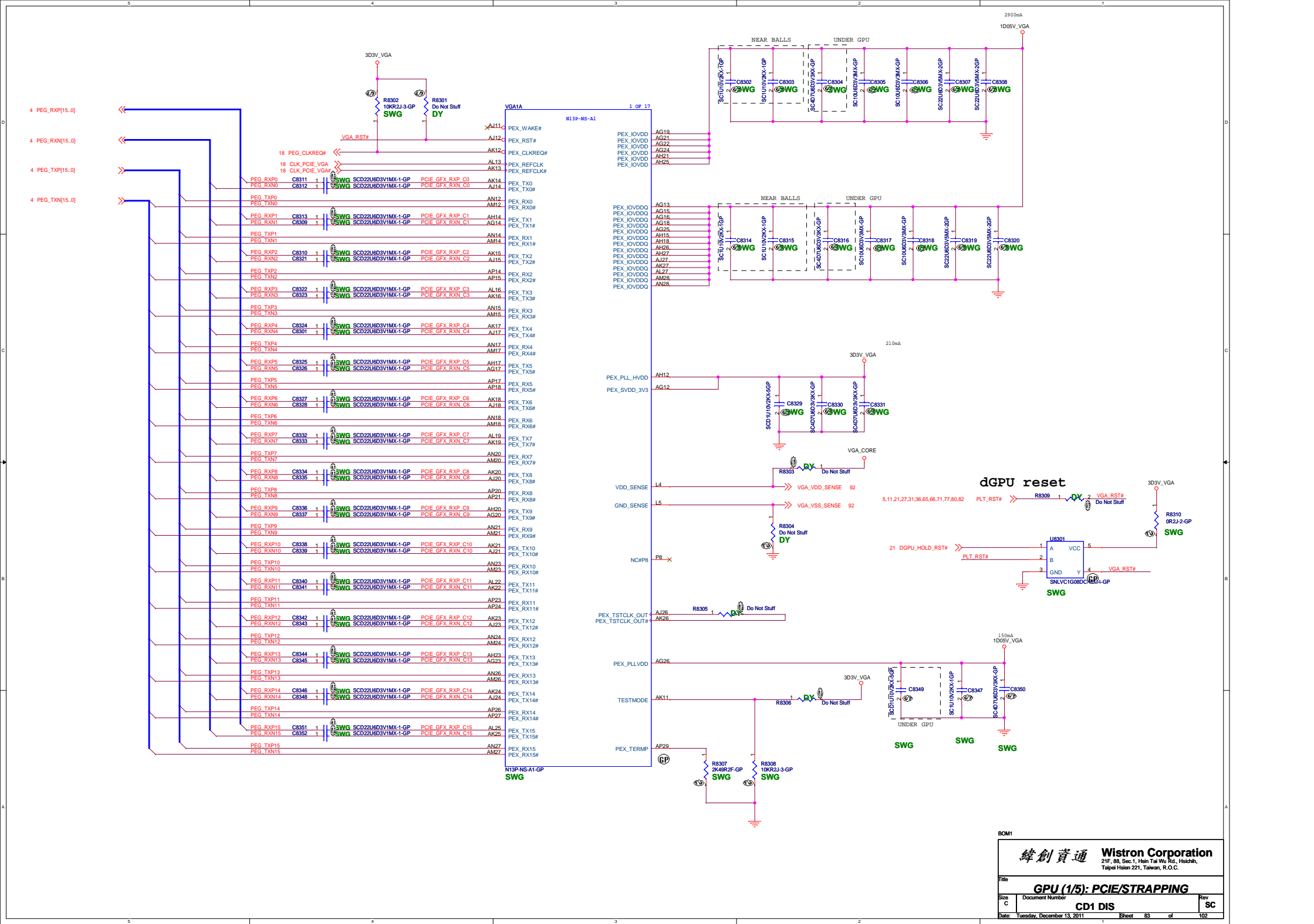
change symbol

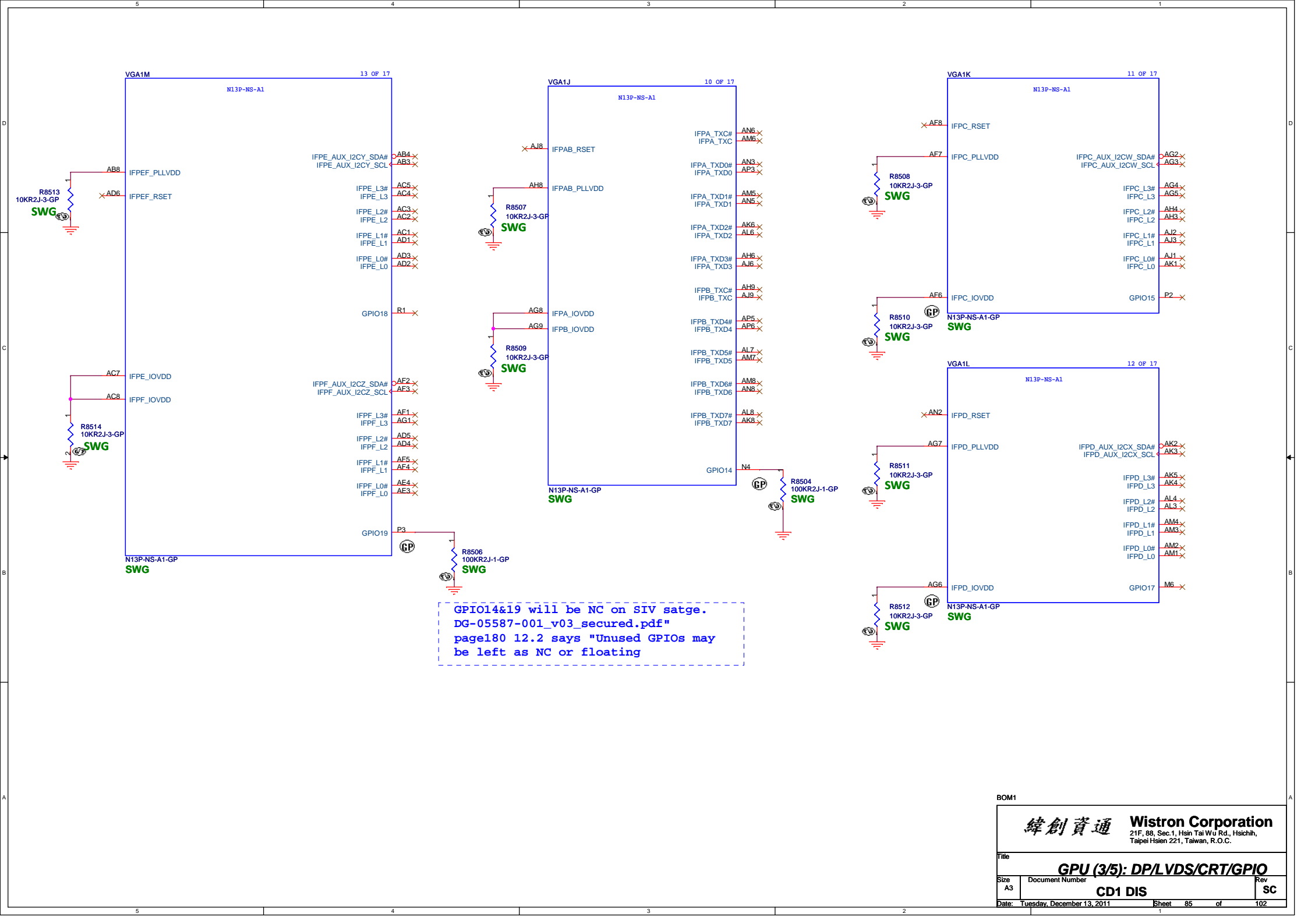


BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

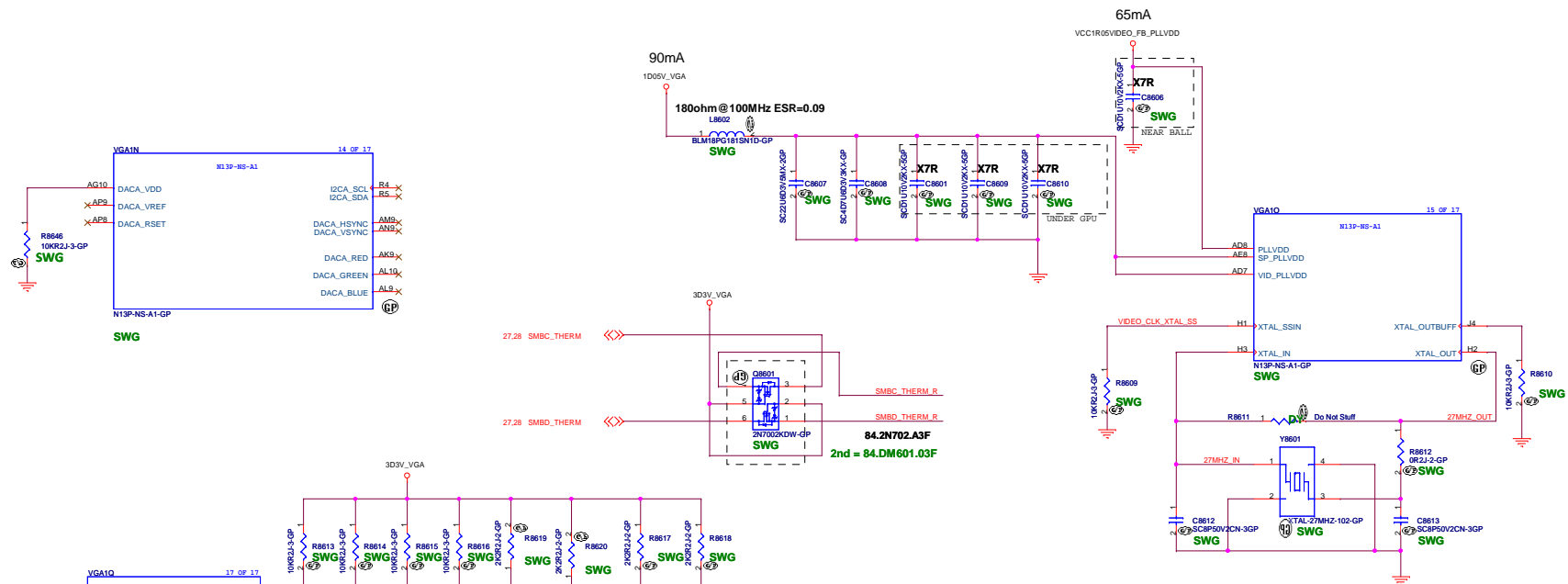
Title			IO Board Connector		
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Title			
GPU (3/5): DP/LVDS/CRT/GPIO			
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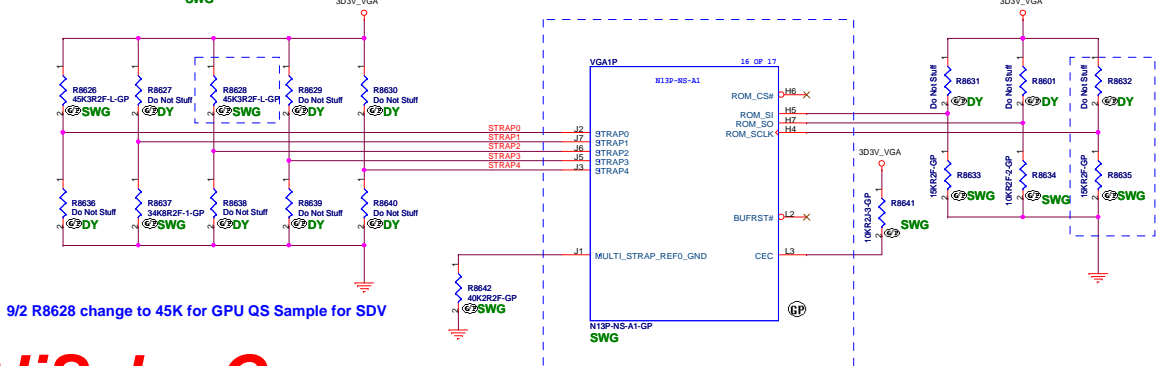


TXC	27MHZ	8.5PF	61Y9503AA
7M27000149	30PPM	4P	
RIVER	27MHZ	8.5PF	61Y9503BA
FCX-04-27000J51421	50PPM	FCX-04	

TABLE VIDEO MEMORY

	HYNIX 1G	HYNIX 2G	SAMSUNG 1G	SAMSUNG 2G
RAM CFG [3:0]	0010	0110	0011	0111
R8633	15K	35.7K	20K	45.3K
Vendor P/N	H5TQ1G63DFR-11C	H5TQ2G63BFR-11C	K4W1G1646G-BC11	K4W2G1646C-HC11
Wistron P/N	72.51G63.H0U	72.52G63.A0U	72.41646.Q0U	72.42164.D0U

9/2: QS Sample Wistron P/N:71.0N13P.D0U , To Define ROM_SCLK & Strap2 in FVT. Need to update in BOM



9/2 R8628 change to 45K for GPU QS Sample for SDV

9/2 DY R8632, R8635 change to Mount for GPU QS Sample for SDV

N13P-ES4-A1	Setting	ROM_SCLK	Strap2
	0x0DEF	0010	1111
		15Kohm pull-down	45Kohm pull-up

緯創資通

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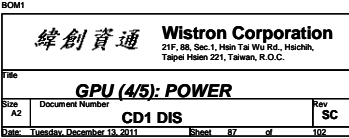
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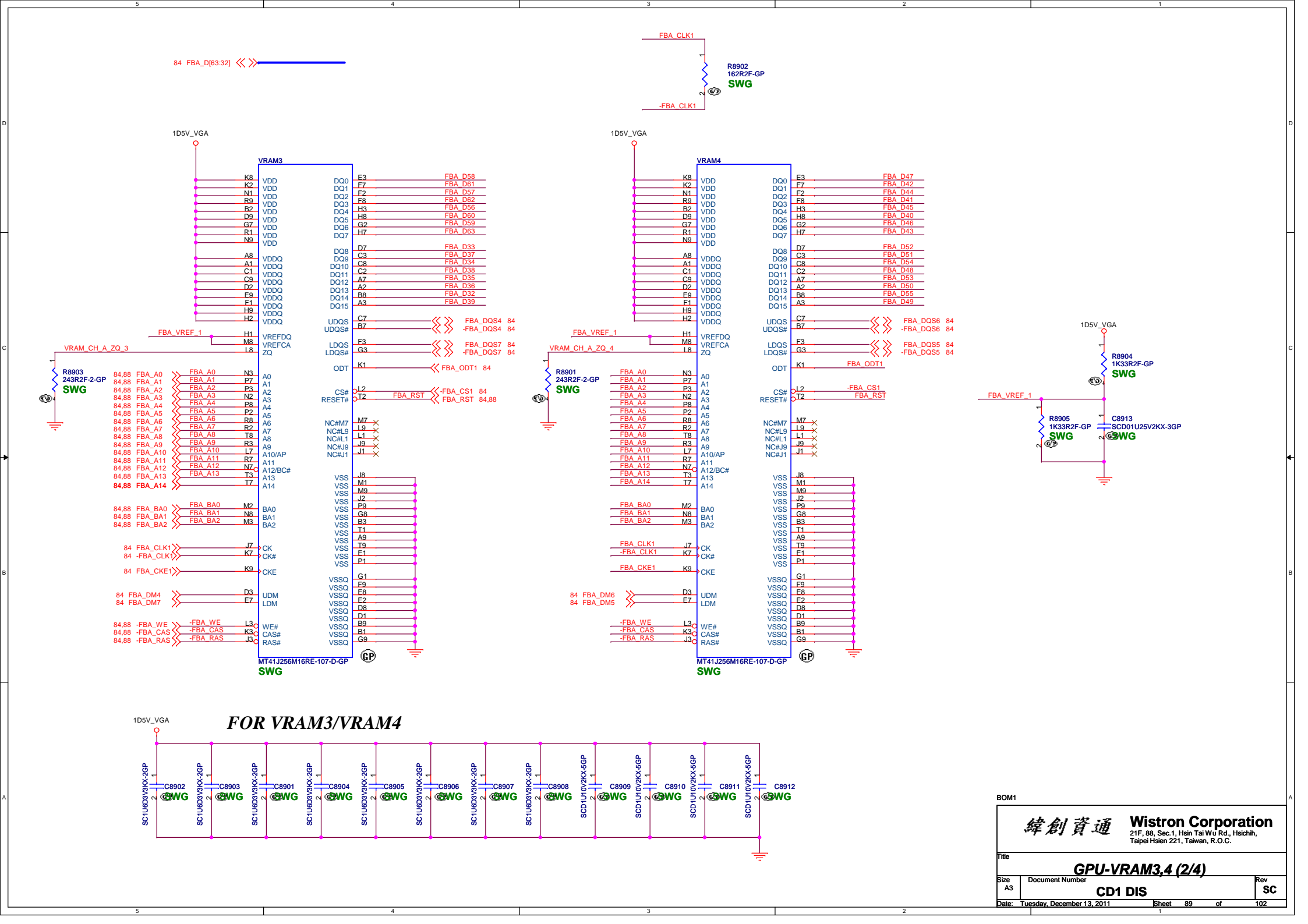
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GPU (5/5): DPPWR/GND

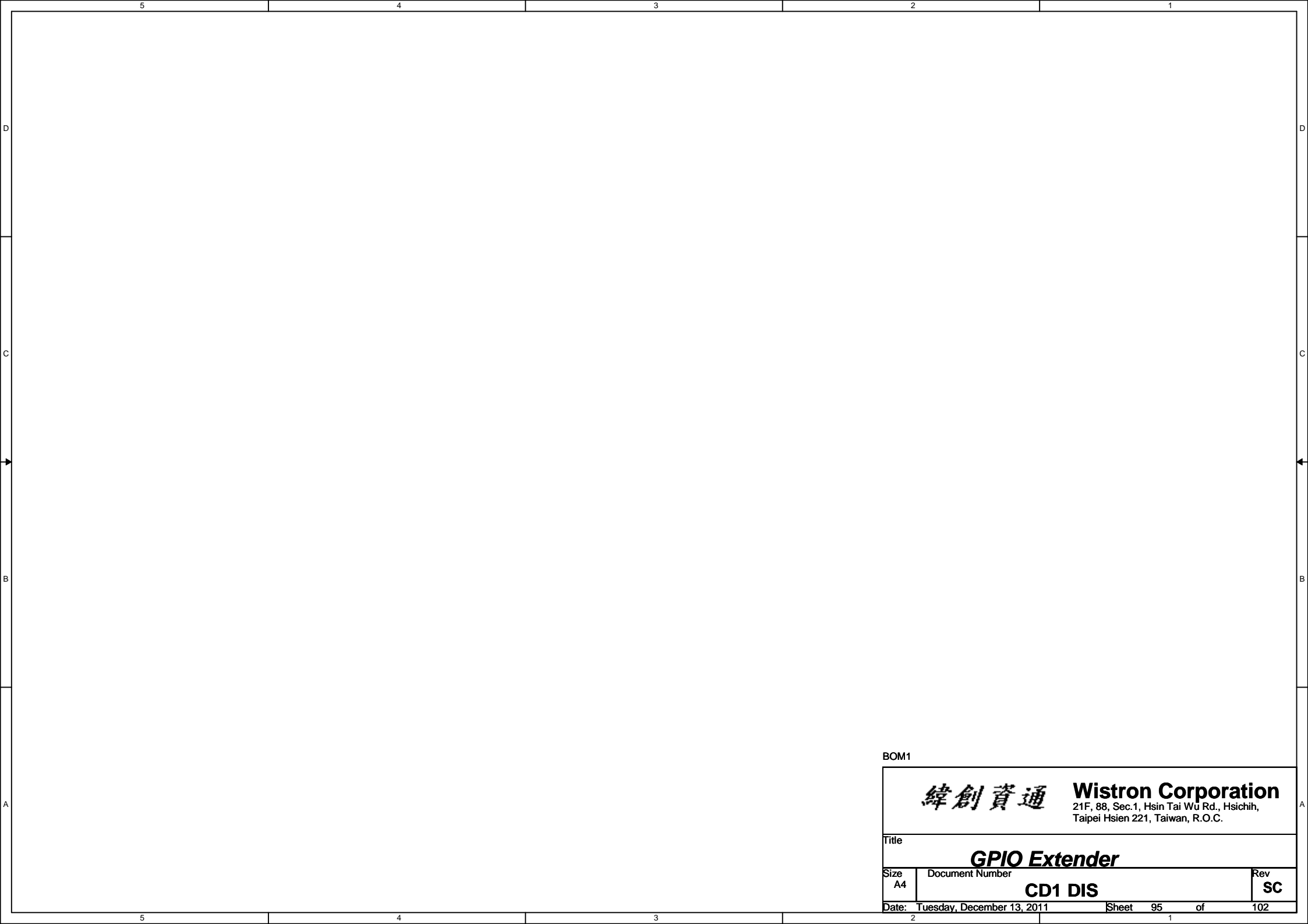
Size A2 Document Number **CD1 DIS** Rev **SC**

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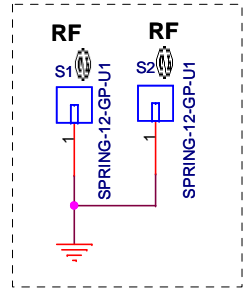
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GPIO Extender	
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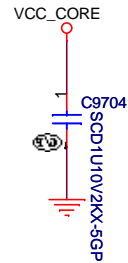
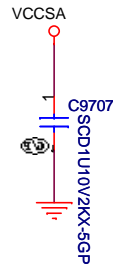
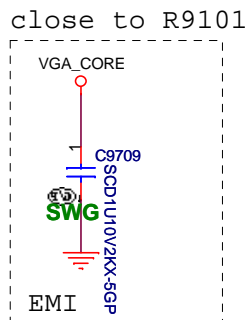
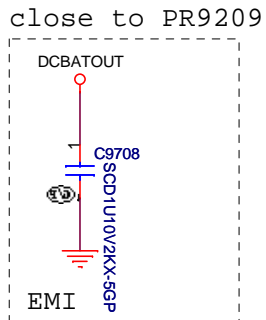
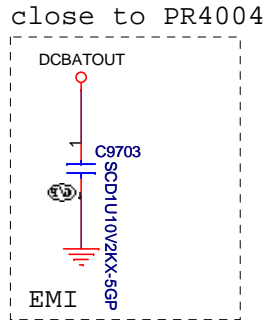
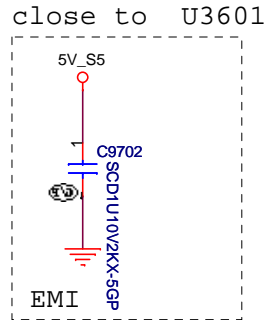
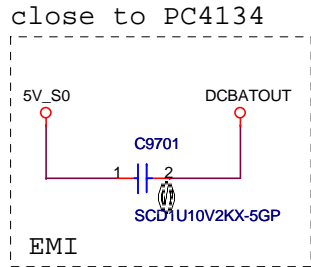
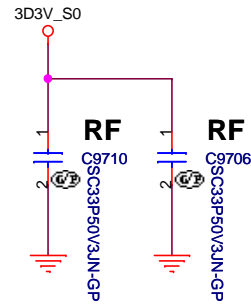
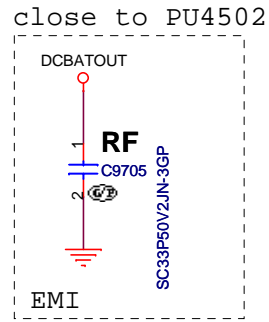
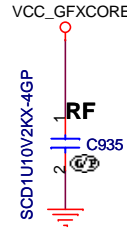
(Blanking)

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Reserved			
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Only for BF UMA
(11270) layout



12/6 RF Solution Table:

Location	CD DIS	CD UMA	BF UMA
C1427 33PF	No_ASM	No_ASM	ASM
EC4601 33PF	ASM	ASM	No_ASM
PC4126 33PF	ASM	ASM	No_ASM
PC4120 33PF	ASM	ASM	No_ASM
PC4613 33PF	ASM	ASM	No_ASM
C9705 33PF	ASM	ASM	No_ASM
PC4622 330PF	ASM	ASM	No_ASM
PR4612 2.2ohm	ASM	ASM	No_ASM
C9710 C9706 33PF	No_ASM	No_ASM	ASM
C935 0.1uF	No_ASM	No_ASM	ASM
S1 S2 Spring	No_ASM	No_ASM	ASM

BOM1

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EMI Capacitors

Size Document Number


Custom **CD1 DIS**

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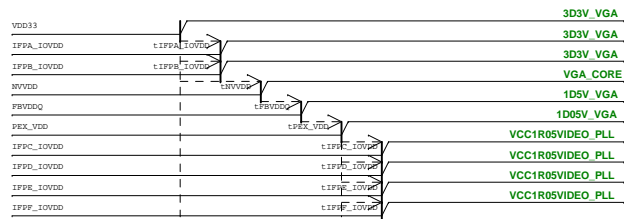
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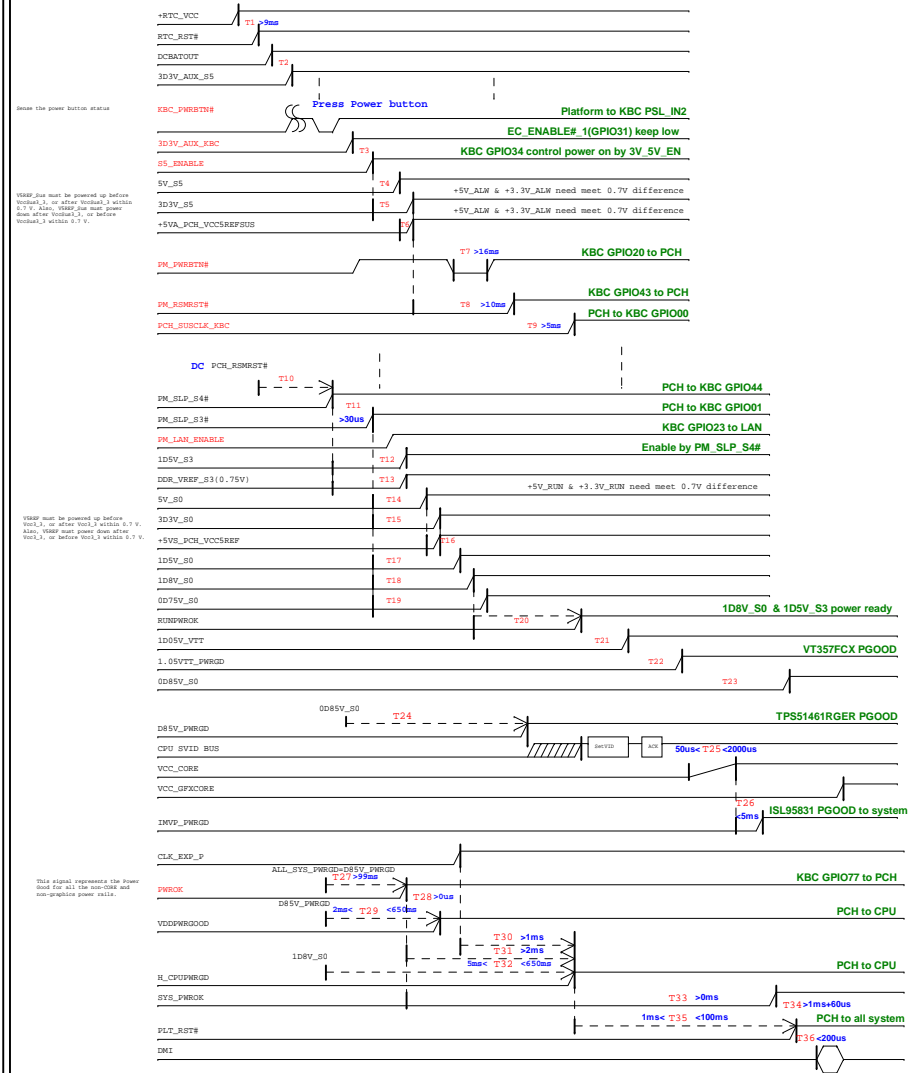
BOM1		 緯創資通 Wistron Corporation 21F, 88, Sec. 1, Main Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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<i>Change History</i>			
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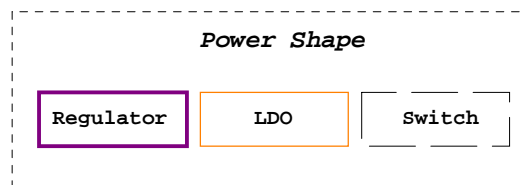
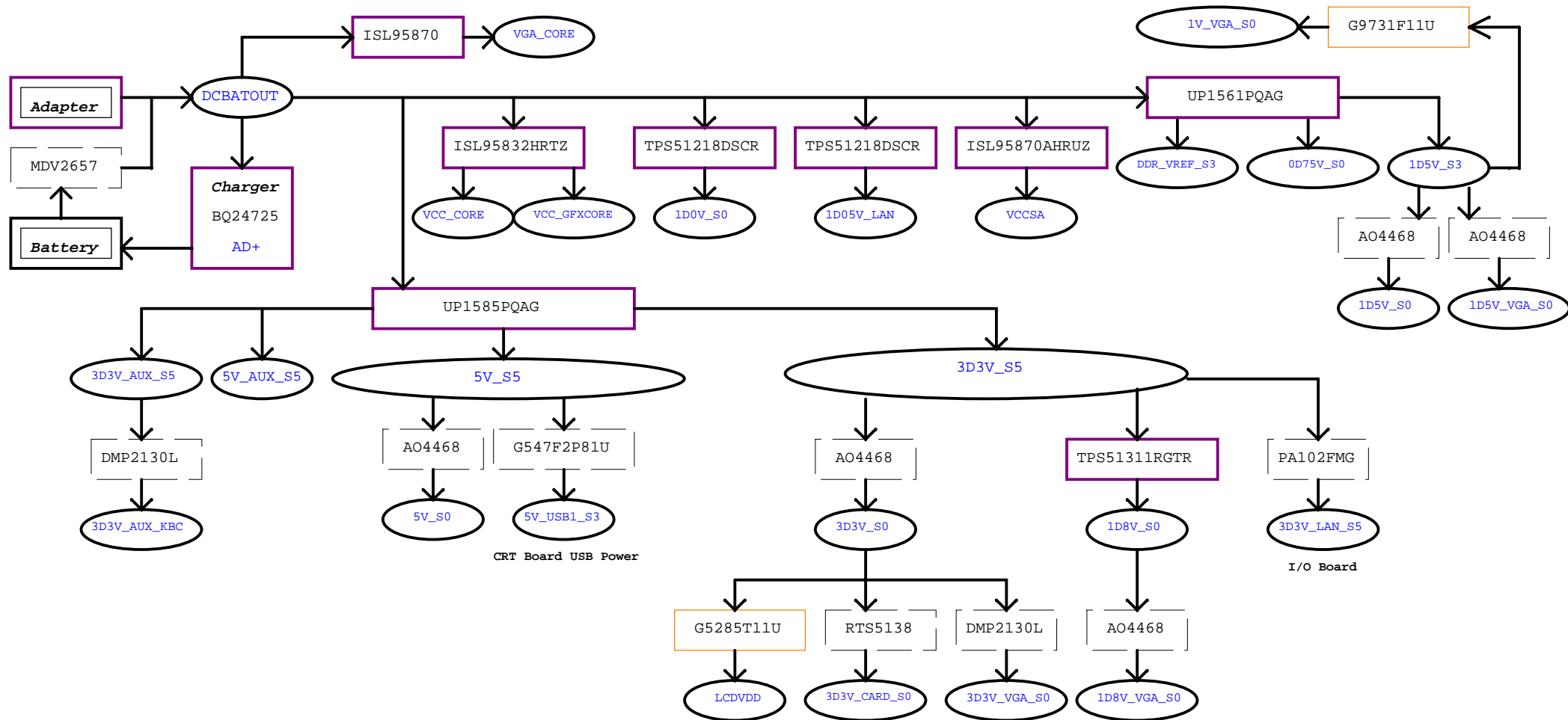
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NVIDIA



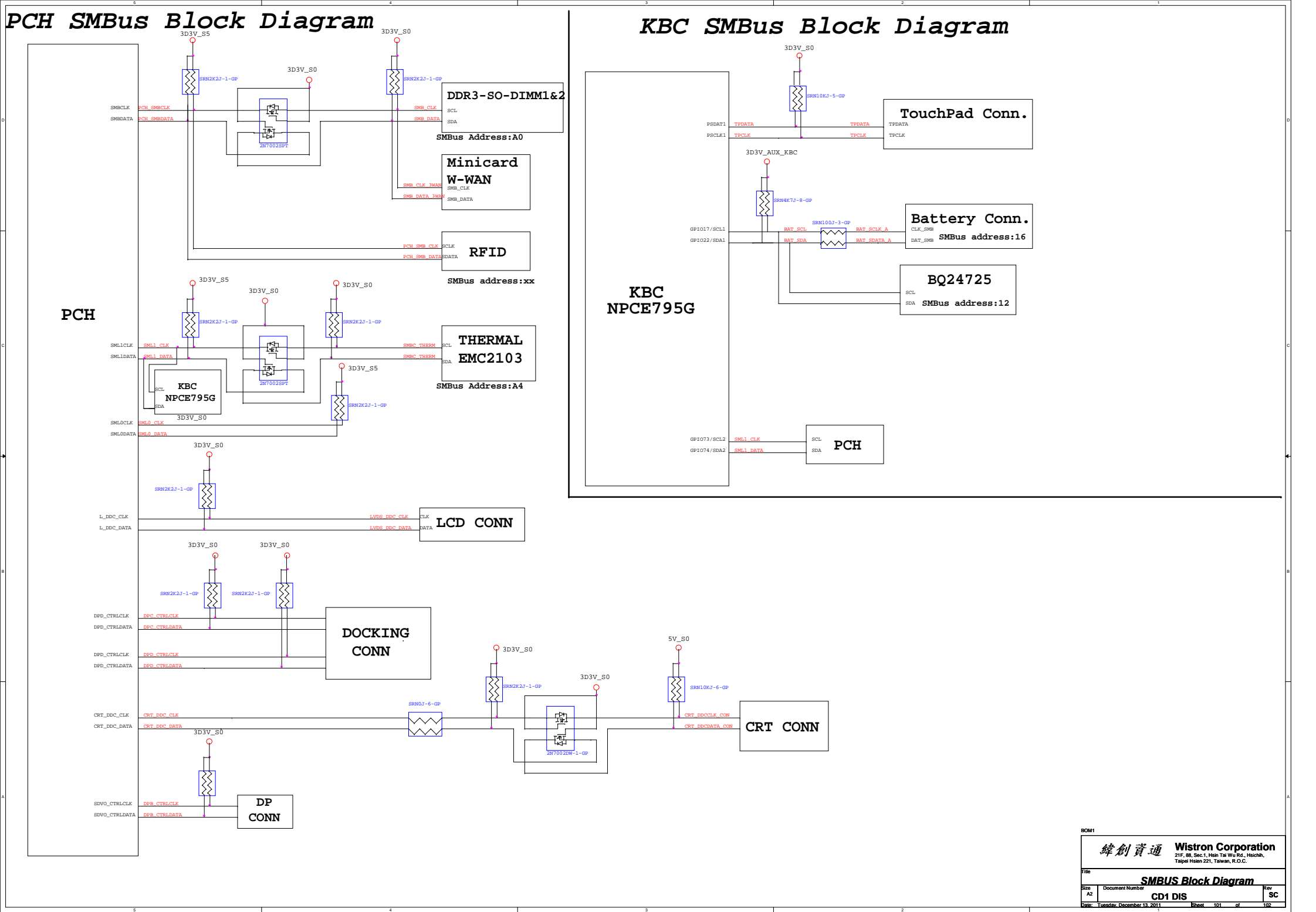
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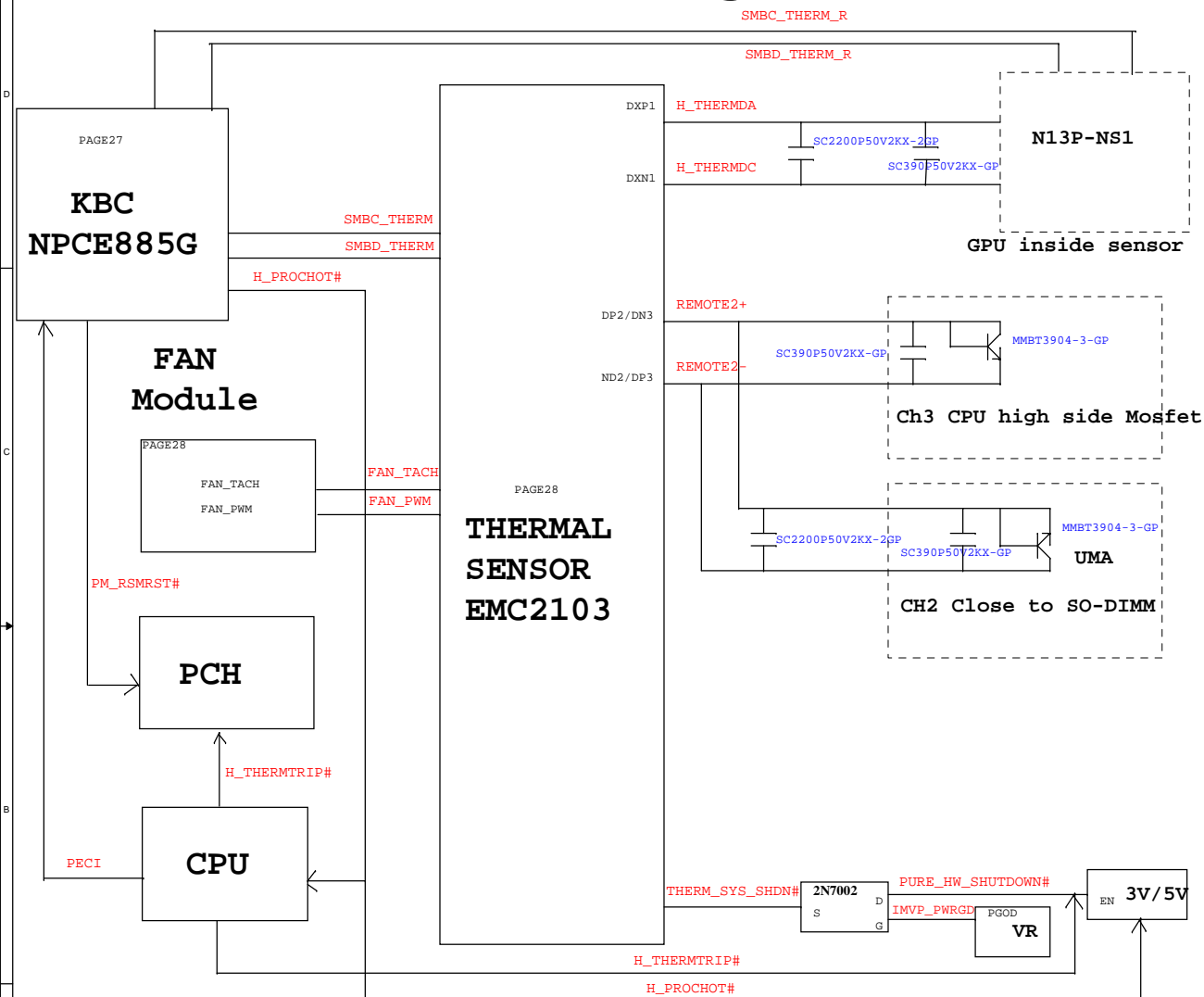


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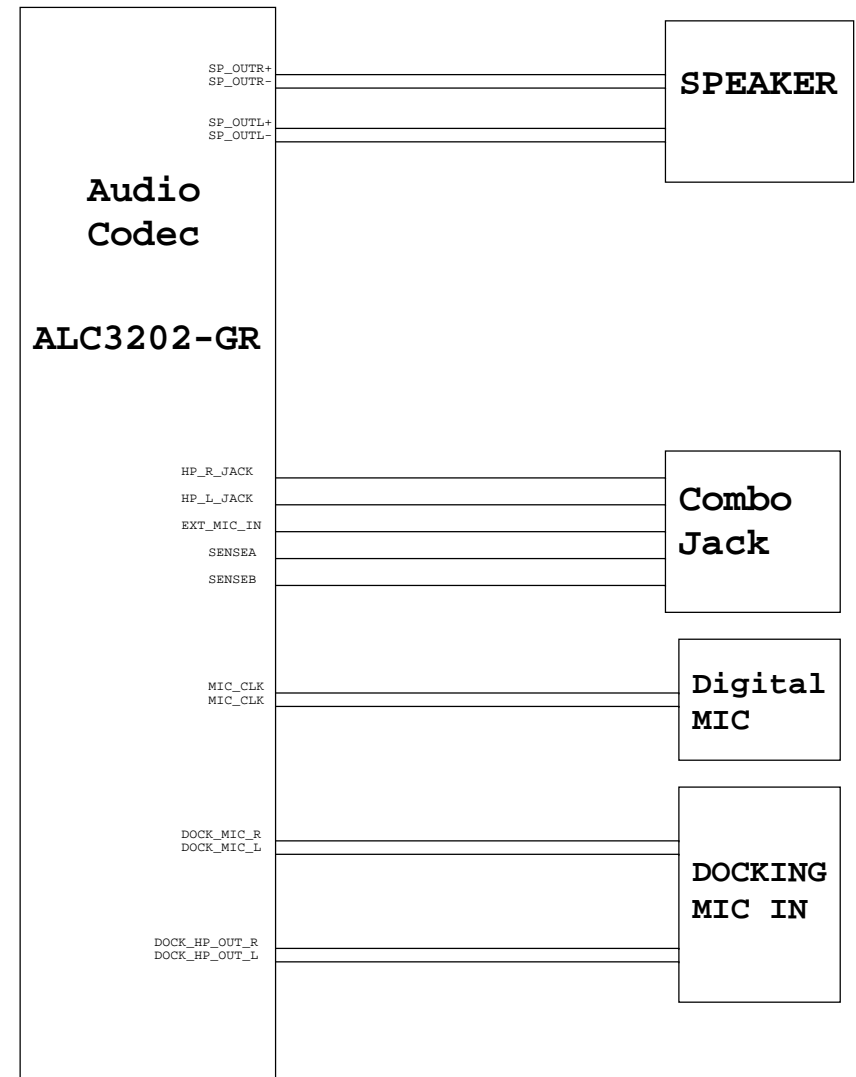
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Title	
Power Block Diagram	
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Thermal Block Diagram



Audio Block Diagram



BOM1

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Thermal/Audio Block Diagram

SC